Improved Voltage Followers

Version 1

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21.07.2026

This notebook presents improved voltage followers including the super source follower (SSF) and the flipped voltage follower (FVF). It looks in particular to the frequency response and stability of these circuits.

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1 Introduction

This notebook studies several voltage followers [1] [2], including the super source follower (SSF) [3] and the flipped voltage follower (FVF) [4] [5] which provide a much lower output resistance than the simple voltage follower (SVF).

All the studied voltage followers will be simulated using ngspice with the EKV 2.6 compact model for a generic 180 nm bulk CMOS technology. The physical parameters are given in Table 1.1, the global process parameters in Table 1.2 and the transistor parameters in Table 1.3.

Table 1.1: Physical parameters

Parameter	Value	Unit
T	300	K
U_T	25.875	mV

Table 1.2: Global process parameters

Parameter	Value	Unit
V_{DD}	1.8	V
C_{ox}	8.443	$\frac{fF}{\mu m^2}$
W_{min}	200	nm
L_{min}	180	nm

Table 1.3: Transistor process parameters

Parameter	NMOS	PMOS	Unit
sEKV parameters			
n	1.27	1.31	-
$I_{spec\square}$	715	173	nA
V_{T0}	0.455	0.445	V
L_{sat}	26	36	nm
λ	13	20	$\frac{V}{\mu m}$
Overlap capacitances parameters			
C_{GDo}	0.366	0.329	$\frac{fF}{\mu m}$
C_{GSo}	0.366	0.329	$\frac{fF}{\mu m}$
C_{GBo}	0	0	$\frac{fF}{\mu m}$
Junction capacitances parameters			
C_J	1	1.121	$\frac{fF}{\mu m^2}$
C_{JSW}	0.2	0.248	$\frac{fF}{\mu m}$
Flicker noise parameters			
K_F	8.1e-24	6.8e-23	J
AF	1	1	-
ρ	0.05794	0.4828	$\frac{V \cdot m^2}{A \cdot s}$

Table 1.3: Transistor process parameters

Parameter	NMOS	PMOS	Unit
Matching parameters			
A_{VT}	5	5	$mV \cdot \mu m$
A_β	1	1	$\% \cdot \mu m$
Source and drain sheet resistance parameter			
R_{sh}	600	2386	$\frac{\Omega}{\mu m}$
Width and length parameters			
ΔW	39	54	nm
ΔL	-76	-72	nm

2 The simple voltage follower (SVF)

2.1 Introduction

(a) SVF in common substrate.

(b) SVF in separate well.

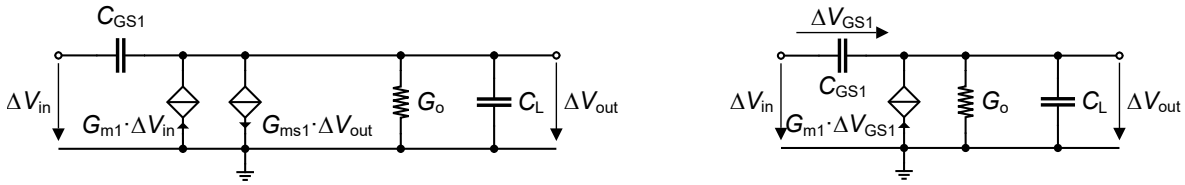
Figure 2.1: Schematics of the SVF.

The schematic of the common-drain or simple voltage follower (SVF) is presented in Figure 2.1. Transistor M_1 can be either in the common substrate as shown in Figure 2.1a, or in a separate well as shown in Figure 2.1b. We will see below that this has an impact of the DC gain.

2.2 Large-signal consideration

The minimum input voltage corresponds to the input voltage at which the output voltage becomes equal to zero. It is then approximately equal to the V_{GS} of M_1 $V_{in,min} \cong V_{GS1}$ which is about equal to V_{T0n} if the transistor is biased in moderate inversion. The maximum input voltage is actually equal to V_{DD}.

2.3 Small-signal transfer function



(a) SVF in common substrate.

(b) SVF in separate well.

Figure 2.2: Small-signal schematics of the SVF.

The small-signal schematic of the SVF are given in Figure 2.2 where G_o is the total conductance at the output (G_{ds1} plus the output conductance of the current mirror). The voltage gain for the SVF with M_1 in common substrate of Figure 2.2 is given by

$$A_v(s) = A_{dc}\,\frac{s/\omega_z + 1}{s/\omega_p + 1}, \tag{2.1}$$

with

$$A_{dc} = \frac{G_{m1}}{G_{ms1} + G_o} \cong \frac{G_{m1}}{G_{ms1}} = \frac{1}{n_1}, \tag{2.2}$$

$$\omega_z = \frac{G_{m1}}{C_{GS1}}, \tag{2.3}$$

$$\omega_p = \frac{G_{ms1} + G_o}{C_L + C_{GS1}} \cong \frac{G_{ms1}}{C_L}, \tag{2.4}$$

where we have assumed that $G_o \ll G_{ms1}, G_{m1}$, $C_{GS1} \ll C_L$ and $G_{ms1} = n_1 \cdot G_{m1}$. We see that the DC gain is about equal to $1/n_1$ which is slightly smaller than 1. This drawback can be circumvented by putting M_1 in a separate well as shown in Figure 2.1b. From the corresponding small-signal circuit of Figure 2.2b, we now get

$$A_{dc} = \frac{G_{m1}}{G_{m1} + G_o} \cong 1, \tag{2.5}$$

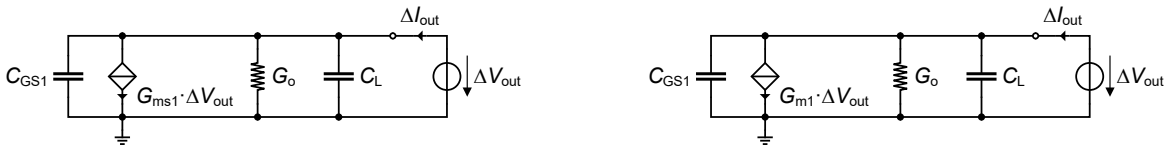
$$\omega_z = \frac{G_{m1}}{C_{GS1}}, \tag{2.6}$$

$$\omega_p = \frac{G_{m1} + G_o}{C_L + C_{GS1}} \cong \frac{G_{m1}}{C_L}, \tag{2.7}$$

At high frequency, the circuit operates like a capacitive divider and the the voltage gain is given by

$$\lim_{s \to +\infty} A_v(s) = \frac{C_{GS1}}{C_L + C_{GS1}} \cong \frac{C_{GS1}}{C_L}. \tag{2.8}$$

2.4 Small-signal output resistance



(a) SVF in common substrate.

(b) SVF in separate well.

Figure 2.3: Small-signal schematics of the SVF for the derivation of the output impedance.

The output impedance of the SVF in common substrate can be calculated wit the help of Figure 2.3a resulting in

$$Z_{out} = \frac{R_{out}}{s/\omega_p + 1}, \tag{2.9}$$

with

$$R_{out} = \frac{1}{G_{ms1} + G_o} \cong \frac{1}{G_{ms1}}. \tag{2.10}$$

In the case M_1 is in a separate well, we get

$$R_{out} = \frac{1}{G_{m1} + G_o} \cong \frac{1}{G_{m1}}. \tag{2.11}$$

2.5 Design

We want to design the SVF in a separate well of Figure 2.4 for the specifications given in Table 2.1.

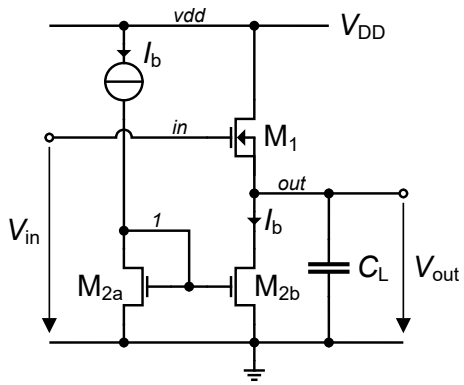


Figure 2.4: Schematic of the SVF used for simulation.

Table 2.1: SVF specifications.

Specification	Symbol	Value	Unit
Minimum bandwidth	BW	1	MHz
Load capacitance	C_L	10	pF

We choose to bias M_1 in moderate inversion with $IC_1 = 1$. We can then calculate the required transconductance $G_{m1} = C_L\,\omega_p = 62.832\ \mu A/V$. The required bias current is then equal to $I_b = G_{m1}\,n\,U_T/gmsid(IC_1) = 3.344\ \mu A$. The I_{spec} and W/L are then given by $I_{spec1} = 3.344\ \mu A$ and $(W/L)_1 = 4.677$. Choosing $L_1 = 1\ \mu m$ we get $W_1 = 4.28\ \mu m$.

The nMOS current mirror is sized with an inversion coefficient $IC_2 = 10$ resulting in $I_{spec2} = 0.334\ \mu A$ and $(W/L)_2 = 0.468$. Choosing $W_2 = W_{min} = 0.20\ \mu m$, we get $L_2 = 0.59\ \mu m$.

The transistor sizing result is summarized in Table 2.2.

Table 2.2: Transistor size and bias information.

Transistor	$W\ [\mu m]$	$L\ [\mu m]$	$I_D\ [\mu A]$	$I_{spec}\ [\mu A]$	IC	$V_G - V_{T0}\ [mV]$	$V_{DSsat}\ [mV]$
M1	4.28	1.00	3.344	3.344	1.0	15	116
M2a	0.20	0.59	3.344	0.334	10.0	130	194
M2b	0.20	0.59	3.344	0.334	10.0	130	194

Table 2.3: Transistor small-signal and thermal noise parameters.

Transistor	$G_{spec}\ [\mu A/V]$	$G_{ms}\ [\mu A/V]$	$G_m\ [\mu A/V]$	$G_{ds}\ [nA/V]$	γ_n
M1	129.252	79.882	62.832	257.261	0.717
M2a	12.925	34.918	27.465	438.290	0.790
M2b	12.925	34.918	27.465	438.290	0.790

2.6 Simulation

We now will simulate the circuit shown in Figure 2.4. We have chosen the input bias voltage in the middle of the supply voltage $V_{inq} = V_{DD}/2 = 0.90\ V$. The operating voltages are given in Table 2.4.

Table 2.4: SVF node voltages.

Node	Voltage
vdd	1.8
in	0.9
out	0.394379
1	0.724485

We can now check the input-output voltage compliance by running a DC sweep. The minimum input voltage can be estmiated to $V_{in,min} = V_{GS1} \cong 0.470\ V$. The simulated large-signal input-output characteristic is plotted in Figure 2.5. It is quite close to the theoretical estimation.

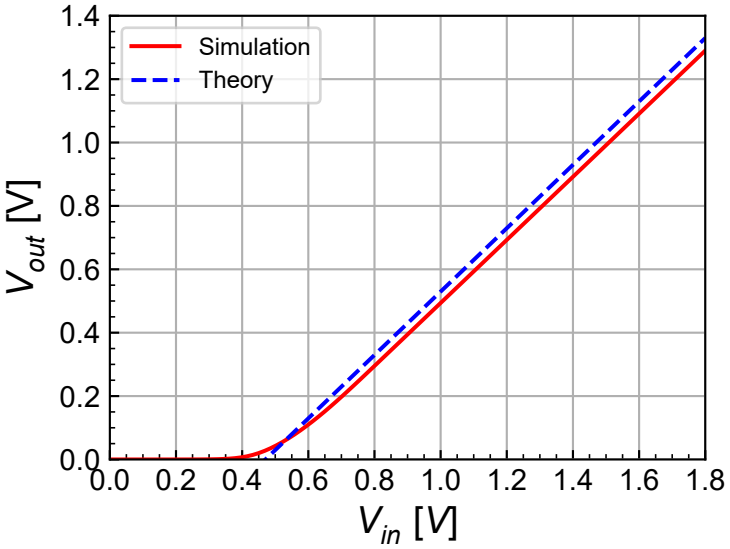


Figure 2.5: Simulated large-signal input-output characteristic.

The small-signal simulated transfer function is compared to the theoretical estimation in Figure 2.6. We see a perfect match between simulation results and theoretical estimation.

Finally, the simulated output impedance normalized to $1/G_{m1}$ is compared to the theoretical estimation in Figure 2.7. Again, we see a perfect match between the simulation and the theoretical estimation.

Voltage followers are used to provide a low output resistance. In the specifications Table 2.1, we have not given any value for this output resistance. The transconductance G_{m1} was actually set by the required bandwidth and corresponds to an output resistance $R_{out} = 15.741\ k\Omega$, which might not be low enough for some applications.

If we need a much lower output resistance of for example $R_{out} = 50\ \Omega$, even for an inversion coefficient as large as $IC_1 = 100$, the required bias current is then $I_b = 6.916\ mA$, which is considerable. We can lower the output resistance compared to the SVF by using one of the improved voltage follower decribed next.

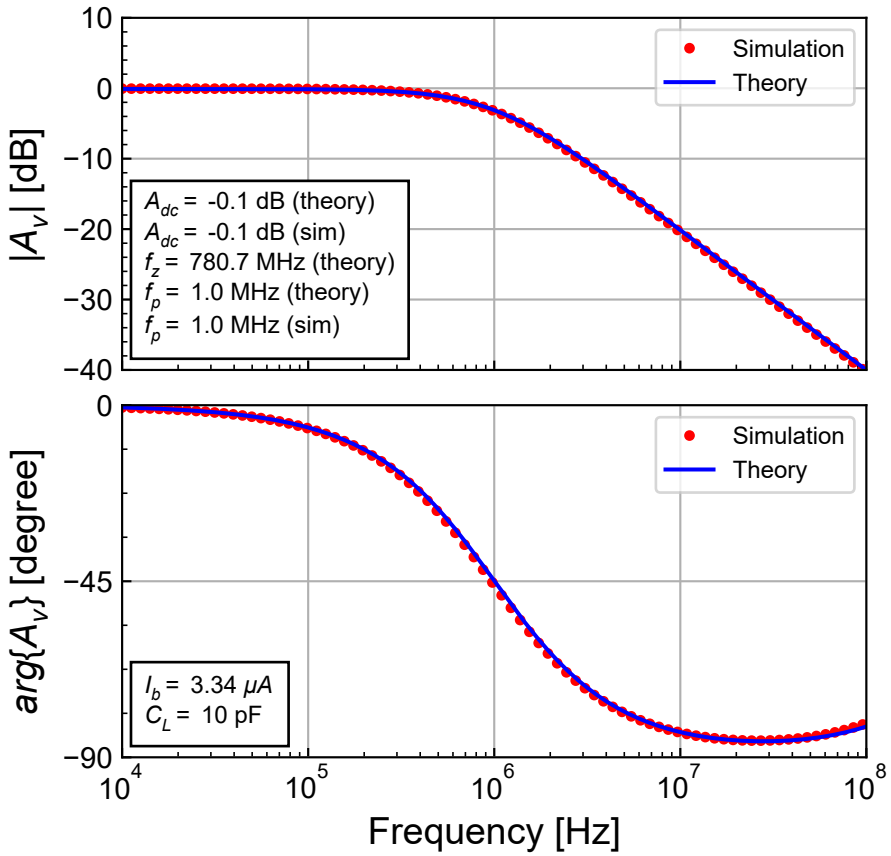


Figure 2.6: Simulated gain response compared to theoretical estimation.

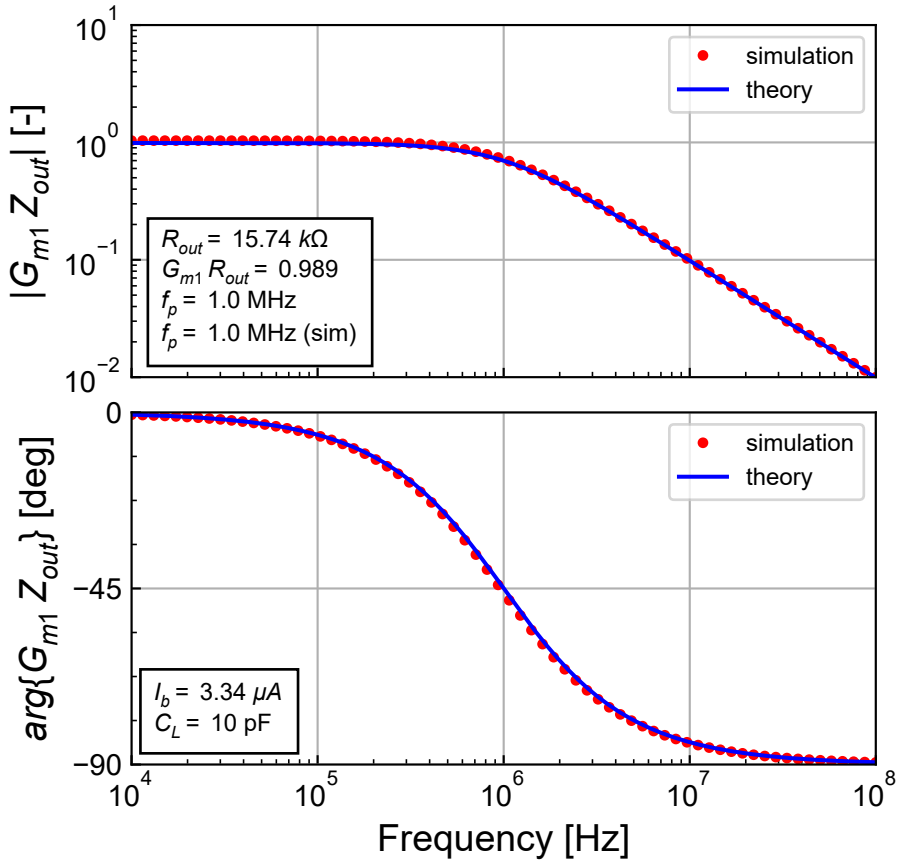


Figure 2.7: Simulated output impedance normalized to $1/G_{m1}$ and compared to the theoretical expression.

3 The super source follower (SSF)

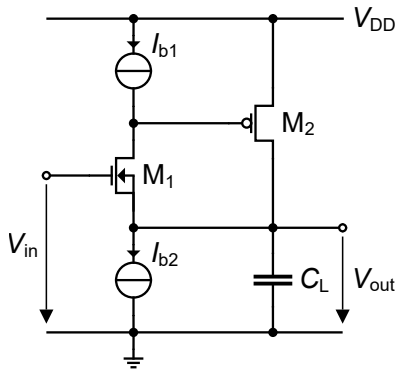


Figure 3.1: Schematic of the SSF [1].

The output resistance of the SVF is limited to $1/G_m$ and might need a high current consumption to have a sufficiently low resistance. This can be circumvented by using the super soource follower (SSF) shown in Figure 3.1 [1]. The SSF introduces a feedback loop with an additional common-source transistor M_2. The feedback loop operates as follows. Let's assume that the ouput voltage increases. For a constant input voltage, the drain current of M_1 decreases and its drain voltage and hence gate voltage of M_2 increases. The drain current of M_2 also decreases and so does its drain voltage bringing the output voltage back to its quiescent value. This means that the feedback loop is trying to keep the output voltage constant, independently of the output current, resulting in a high output resistance. This feature will be analyzed in more details in the next Section.

3.1 Output resistance

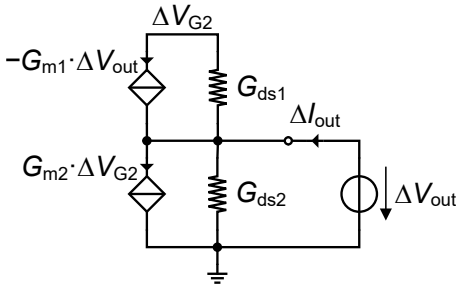


Figure 3.2: Small-signal schematic of the SSF for calculation of the output resistance.

The output resistance can be calculated using the small-signal circuit shown in Figure 3.2, resulting in

$$R_{out} = \frac{G_{ds1}}{G_{m1}\,G_{m2} + G_{m2}\,G_{ds1} + G_{ds1}\,G_{ds2}} \cong \frac{G_{ds1}}{G_{m1}\,G_{m2}} \quad \text{for } G_{ds1} \ll G_{m1} \text{ and } G_{ds2} \ll G_{m2}. \tag{3.1}$$

The output resistance of the SSF is equal to that of the SVF divided by G_{m2}/G_{ds1}.

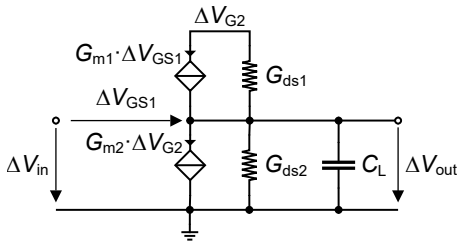


Figure 3.3: Small-signal schematic of the SSF for calculation of the output resistance.

3.2 Transfer function

The voltage gain ignoring all the parasitic capacitance except the load capacitance can be calculated using the small-signal schematic shown in Figure 3.3. This results in

$$A_v(s) = \frac{A_{dc}}{s/\omega_p + 1}, \tag{3.2}$$

with

$$A_{dc} = \frac{G_{m1}\,G_{m2}}{G_{m1}\,G_{m2} + G_{m2}\,G_{ds1} + G_{ds1}\,G_{ds2}} \cong 1, \tag{3.3}$$

$$\omega_p = \frac{G_{m1}\,G_{m2} + G_{m2}\,G_{ds1} + G_{ds1}\,G_{ds2}}{G_{ds1}\,C_L} \cong \frac{G_{m1}\,G_{m2}}{G_{ds1}\,C_L}. \tag{3.4}$$

We see that the bandwidth of the SSF is extended by G_{m2}/G_{ds1} compared to that of the SVF.

To check the above observations, we now will design a SSF for the same specifications than used for the SVF which are repeated in Table 4.1.

Table 3.1: FVF specifications.

Specification	Symbol	Value	Unit
Minimum bandwidth	BW	1	MHz
Load capacitance	C_L	10	pF

The circuit requires a minimum supply voltage equal to two saturation voltages and one V_{GS} voltage. In order to save some voltage headroom, we choose to bias M_1 and M_2 in moderate inversion with $IC_1 = IC_2 = 1$.

We will use the same current I_b of the SVF to bias M_1 $I_{D1} = I_b = 3.344\ \mu A$. This results in the same transconductance as used for M_1 in the SVF, namely $G_{m1} = 62.832\ \mu A/V$. The specific current and W/L ratio are then given by $I_{spec1} = 3.344\ \mu A$ and $(W/L)_1 = 4.677$. To have enough self-gain we choose a long transistor with $L_1 = 1.00\ \mu m$, resulting in $W_1 = 4.28\ \mu m$. M_1 is therefore identical to M_1 of the SVF.

We decide to use the same bias current for M_2 $I_{D2} = I_{D1} = 3.344\ \mu A$. The transconductance is then given by $G_{m2} = I_{D2}/(n_{0p}\,U_T) = 61.164\ \mu A/V$. The specific current and W/L ratio are then given by $I_{spec2} = 3.344\ \mu A$ and $(W/L)_2 = 19.317$. Since the W/L of M_2 is much larger than that of M_1, we choose a slightly shorter length $L_2 = 0.50\ \mu m$, we get $W_2 = 8.21\ \mu m$.

The transistor sizing result is summarized in Table 4.2, while the small-signal parameters are given in Table 4.3.

Table 3.2: Transistor size and bias information.

Transistor	$W\ [\mu m]$	$L\ [\mu m]$	$I_D\ [\mu A]$	$I_{spec}\ [\mu A]$	IC	$V_G - V_{T0}\ [mV]$	$V_{DSsat}\ [mV]$
M1	4.28	1.00	3.344	3.344	1.0	15	116
M2	8.21	0.50	3.344	3.344	1.0	15	116

Table 3.3: Transistor small-signal and thermal noise parameters.

Transistor	$G_{spec}\ [\mu A/V]$	$G_{ms}\ [\mu A/V]$	$G_m\ [\mu A/V]$	$G_{ds}\ [nA/V]$	γ_n
M1	129.252	79.882	62.832	257.261	0.717
M2	129.252	79.882	61.164	334.439	0.736

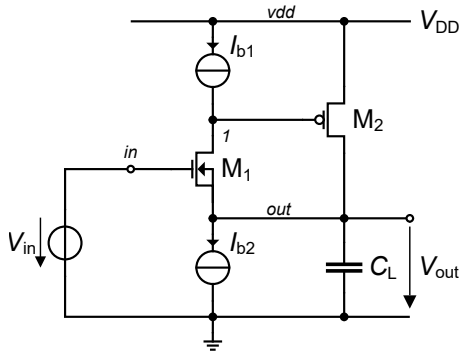


Figure 3.4: Schematic of the SSF used for simulation.

We now will simulate the circuit shown in Figure 3.4. We have chosen the input bias voltage $V_{inq} = 0.90\ V$. The operating voltages are given in Table 4.4.

Table 3.4: FVF node voltages.

Node	Voltage
vdd	1.8
in	0.9
out	0.392301
1	1.28649

The operating point looks fine. We can now proceed with the simulation of the voltage gain with an AC simulation. The result is shown in Figure 4.4. We can check the large- and small-signal parameters which are extracted from the operating point file and presented in Table 3.5 and Table 3.6.

Table 3.5: Large-signal operating point information extracted from ngspice .op file for each transistor.

Transistor	$I_D\ [\mu A]$	$I_{spec}\ [\mu A]$	IC [-]	n [-]	$V_{DSsat}\ [mV]$
M1	3.344	3.303	1.015	1.27	156
M2	3.345	3.424	0.981	1.31	155

Table 3.6: Small-signal operating point information extracted from ngspice .op file for each transistor.

Transistor	G_m $[\mu A/V]$	G_{ms} $[\mu A/V]$	G_{ds} $[nA/V]$
M1	61.325	78.778	119.879
M2	60.342	80.315	165.222

We see that the simulated transconductances are slightly smaller than the one derived in the design phase.

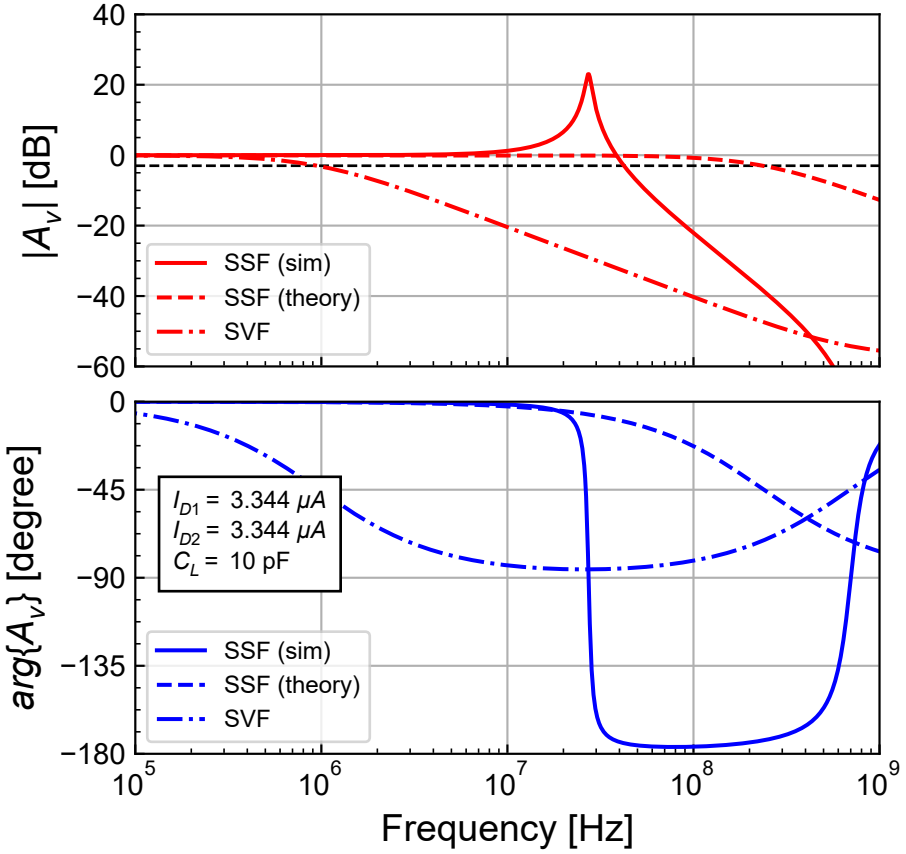


Figure 3.5: Simulated gain response compared to theoretical estimation.

From Figure 3.5, we see that the bandwidth has been increased by almost a factor 30 compared to the SVF for the same load capacitance! However, we see that the transfer function shows some big peaking at about 20 MHz and a steeper roll-off of -40 dB/dec indicating that the transfer function is of 2nd-order with a Q-factor larger than 1. This can be dangerous in terms of stability. We need to have a closer look at this.

The 2nd-order transfer function is coming from the additional parasitic capacitances at the drain node of M_1 which we have intentionnally ignored. Let's now derive the expression of the voltage gain accounting for these parasitic capacitances. The small-signal schematic including the parasitic capacitances C_{p1} and C_{p2} is shown in Figure 3.6. Note that the parasitic capacitance C_{p1} is connected between the drain and the bulk of M_1 which is also the source terminal since M_1 is in a separate well.

The voltage gain including the parasitic capacitances C_{p1} and C_{p2}, but assuming that $C_L \gg C_{p1}, C_{p2}$ and $G_{ds1} \ll G_{m1}$ and $G_{ds2} \ll G_{m2}$, is then given by

$$A_v(s) = A_{dc} \frac{\frac{s}{\omega_z} + 1}{\left(\frac{s}{\omega_0}\right)^2 + \frac{s}{\omega_0 Q} + 1} \tag{3.5}$$

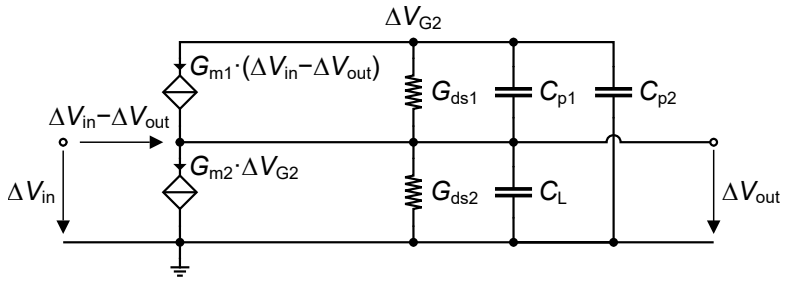


Figure 3.6: Small-signal schematic of the SSF including the parasitic capacitances C_{p1} and C_{p2}.

with

$$A_{dc} \cong 1, \tag{3.6}$$

$$\omega_z = \frac{G_{m2}}{C_{p2}}, \tag{3.7}$$

$$\omega_0 \cong \sqrt{\frac{G_{m1}\, G_{m2}}{C_L\,(C_{p1}+C_{p2})}}, \tag{3.8}$$

$$Q \cong \frac{\sqrt{C_L\,(C_{p1}+C_{p2})\, G_{m1}\, G_{m2}}}{C_L\, G_{ds1} + C_{p2}\, G_{m1} + C_{p1}\, G_{m2}}. \tag{3.9}$$

We now have indeed a 2$^{\text{nd}}$-order low-pass tranfer function with an additional zero in the LHS. To evaluate the transfer function given by (3.5), we need to estimate the parasitic capacitances C_{p1} and C_{p2}. This can be done with the help of Figure 3.7.

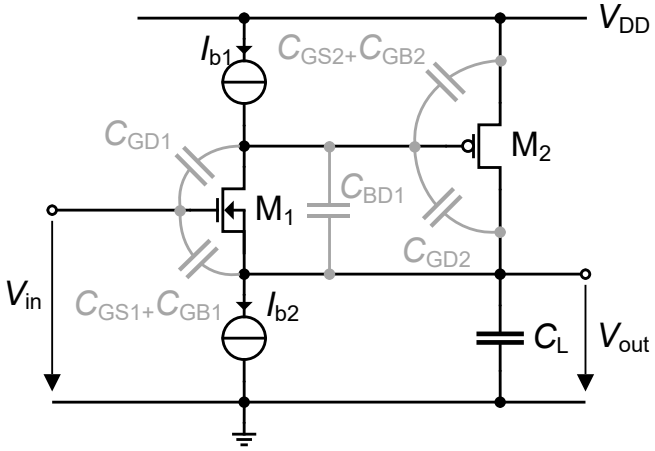


Figure 3.7: Parasitic capacitances associated to M_1 and M_2.

The parasitic capacitance C_{p1} between the drain and soure/bulk of M_1 is given by

$$C_{p1} = C_{BD1} + C_{GD2}, \tag{3.10}$$

where C_{BD1} is the junction capacitance at the drain of M_1 given by

$$C_{BD1} = 2H_{dif} \cdot W_{eff1} \cdot C_{Jn} + 2(2H_{dif} + W_{eff1}) \cdot C_{JSWn}, \tag{3.11}$$

with C_{Jn} the bottom junction capacitance per unit area, C_{JSWn} the side-wall capacitance per unit length and H_{dif} the half minimum diffusion width, which is imposed by the layout rules. Of course the junction capacitances per area and per length C_{Jn} and C_{JSWn} are bias dependent since they depend on the drain-to-bulk voltage, but we consider their highest value obtained for a zero drain-to-bulk voltage (worst case).

C_{GD2} is the gate-to-drain capacitance of M_2. Since M_2 is in saturation, the intrinsic capacitance can be neglected and C_{GD2} is given by

$$C_{GD2} = W_{eff2}\, C_{GDe}. \tag{3.12}$$

where C_{GDe} is the extrinsic capacitance per unit width which includes the overlap and fringing field capacitance and is given by

$$C_{GDe} = C_{GDo} + C_{GDf}. \tag{3.13}$$

where C_{GDo} is the overlap capacitance per unit width and C_{GDf} is the fringing field capacitance per unit width. Note that for the chosen 180 nm technology, the fringing capacitance per unit width C_{GDf} is actually zero.

The parasitic capacitance C_{p2} between the drain of M_1 and ground is given by

$$C_{p2} = C_{GD1} + C_{GS2} + C_{GB2}, \tag{3.14}$$

C_{GD1} is the extrinsic capacitance given by

$$C_{GD1} = W_{eff1}\, C_{GDe}. \tag{3.15}$$

C_{GS2} is made of the intrinsic and extrinsic capacitance according to

$$C_{GS2} = W_{eff2}\, L_{eff2}\, C_{ox}\, c_{gsi} + W_{eff2}\, C_{GDe}, \tag{3.16}$$

where c_{gsi} is the normalized intrinsic capacitance which depends on bias, but becomes negligible in moderate and weak inversion. We therefore will neglect the intrinsic part of C_{GS2}.

C_{GB2} is the gate-to-bulk capacitance which is usually made of an intrinsic and extrinsic capacitance

$$C_{GB2} = W_{eff2}\, L_{eff2}\, C_{ox}\, c_{gbi} + W_{eff2}\, C_{GBe}, \tag{3.17}$$

where c_{gbi} is the normalized gate-to-bulk intrinsic capacitance which depends on bias and C_{GBe} is the gate-to-bulk extrinsinc capacitance which is mostly the overlap capacitance. Note that in this technology the gate-to-bulk overlap capacitance is almost negligible.

We can now compute all the small-signal parameters in order to compute the theoretical transfer function given by (3.5). They are presented in Table 3.7.

Table 3.7: Estimation of the small-signal parameters.

Parameter	Value	Unit
G_{m1}	62.832	$\mu A/V$
G_{m2}	61.164	$\mu A/V$
G_{ds1}	257.261	nA/V
G_{ds2}	334.439	nA/V
G_{m1}/G_{ds1}	244.234	-
G_{m1}/G_{ds1}	47.756	dB
G_{m2}/G_{ds2}	182.885	-
G_{m2}/G_{ds2}	45.244	dB
C_{BD1}	2.673	fF
C_{GD2}	2.698	fF
C_{p1}	5.371	fF
C_{GD1}	1.57	fF
C_{GS2}	2.698	fF
C_{GB2}	4.667	fF
C_{p2}	8.935	fF

Table 3.7: Estimation of the small-signal parameters.

Parameter	Value	Unit
A_{dc}	1	-
A_{dc}	0	dB
f_z	1089.51	MHz
f_0	26.085	MHz
Q	6.772	-

We see that the resonance frequency is now $f_0 = 26.085\ MHz$ and the quality factor is $Q = 6.772$, which is indeed larger than one explaining the peaking. We can now compare the simulated transfer function to the theoretical one given by (3.5) calculated with the small-signal parameters given in Table 3.7. The result is shown in Figure 4.5.

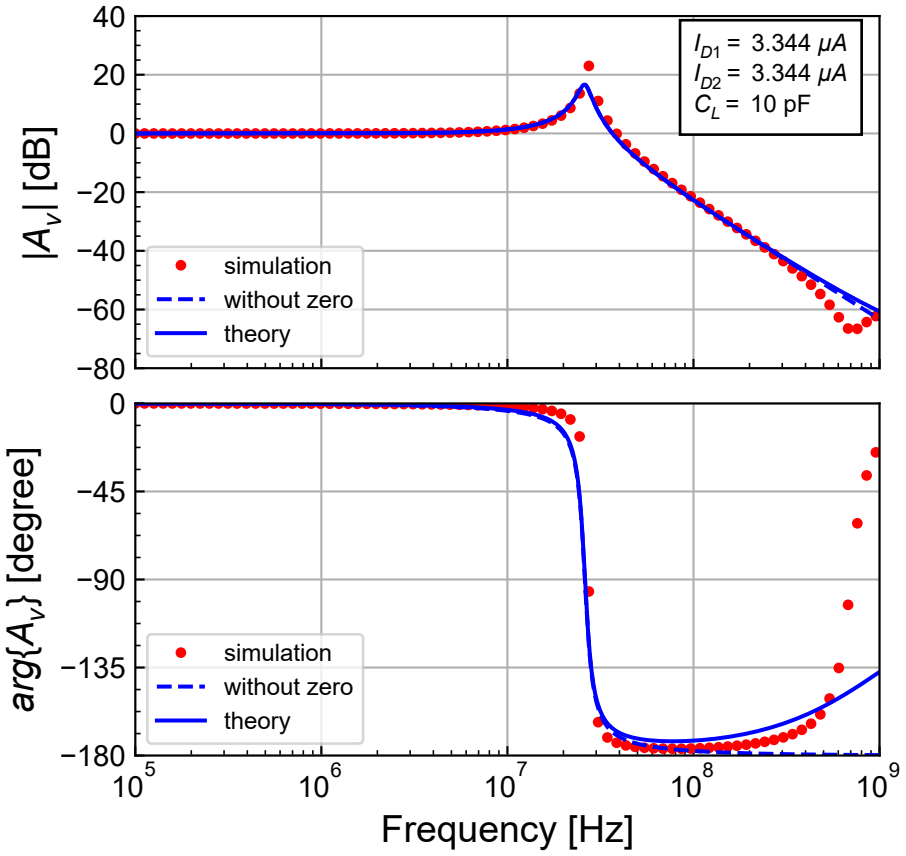


Figure 3.8: Simulated gain response compared to theoretical estimation.

We see that the theoretical transfer function given by (3.5) matches the simulaton result reasonably well. From Table 3.7, we see that the zero frequency $f_z = 1089.509$ MHz is way above the resonance frequency $f_0 = 26.085$ MHz and can therefore be neglected. This approximation with $\omega_z \to \infty$ is shown by the dashed lines in Figure 3.8.

In many applications the peaking shown in Figure 3.8 is not acceptable. The step response will oscillate as shown in Figure 3.9 and the settling time might be even longer than what is obtained by the SVF.

We now will try to better understand the issue by analyzing the circuit using feedback theory.

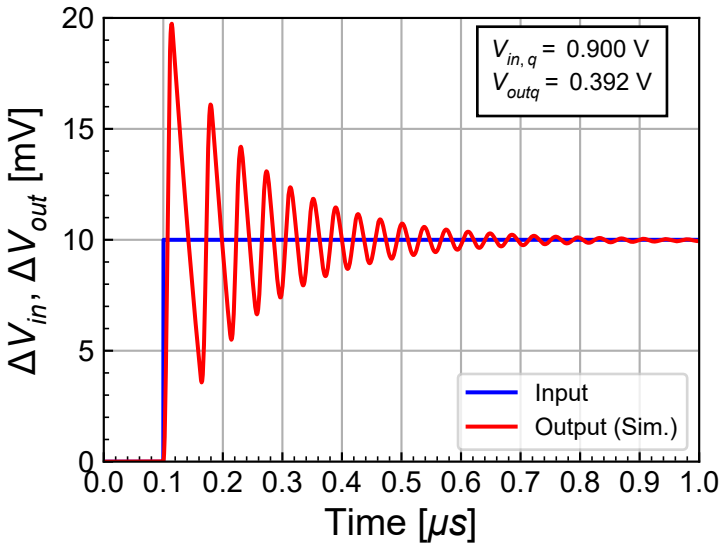
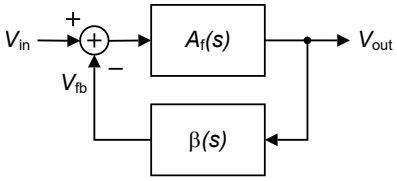


Figure 3.9: FVF step response.

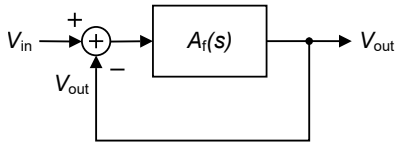
3.3 Feedback analysis

The SSF can be viewed as a general feedback system as shown in Figure 3.10a with the feedback applied directly at the source of M_1. If we now look at the small-signal schematic of Figure 3.6, we see that the difference between the input and output voltage is perfomed at the input of transconductor G_{m1}. We can therefore represent this circuit as a feedback system with a feedback gain $\beta = 1$ as shown in Figure 3.10b. Since $\beta = 1$, $A_f(s)$ is also equal to the loop gain $L(s)$. The closed-loop gain is then given by

$$A_v(s) = \frac{A_f(s)}{1 + A_f(s)}. \tag{3.18}$$



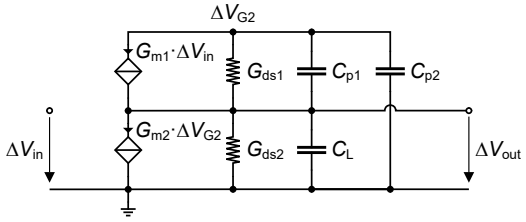
(a) General feedback system.



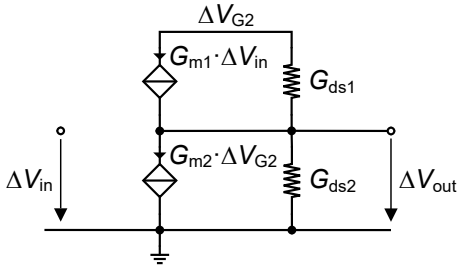
(b) SSF as a feedback system.

Figure 3.10: The SSF as a feedback system.

To calculate the forward gain $A_f(s)$, we can *virtually* open the loop by setting $\Delta V_{out} = 0$ in the control voltage of G_{m1}. The feedback is then disabled and we can now calculate the forward gain $A_f(s)$ with the help of the circuit shown Figure 3.11.



(a) With capacitances



(b) DC.

Figure 3.11: Small-signal circuit to calculate the forward gain.

We can start calculating the foward gain at DC with the help of the small-signal circuit shown in Figure 3.11b, which results in

$$A_f(0) = \frac{G_{m1}\, G_{m2}}{G_{ds1}\,(G_{m2} + G_{ds2})} \cong \frac{G_{m1}}{G_{ds1}}. \tag{3.19}$$

The closed-loop DC gain is then given by

$$A_{dc} = \frac{G_{m1}\, G_{m2}}{G_{m1}\, G_{m2} + G_{ds1}\,(G_{m2} + G_{ds2})} \cong 1 \quad \text{for } G_{m1} \gg G_{ds1} \text{ and } G_{m2} \gg G_{ds2}. \tag{3.20}$$

If we now account for the capacitances assuming that $C_L \gg C_{p1}, C_{p2}$, we can derive the forward transfer function which is also the loop gain as

$$A_f(s) = L(s) \triangleq \frac{\Delta V_{out}}{\Delta V_{in}} = A_{f,dc}\, \frac{1 + s/\omega_z}{(1 + s/\omega_{p1})\,(1 + s/\omega_{p2})}. \tag{3.21}$$

The parameters can be derived assuming that the poles are sufficiently widely spaced (i.e. $\omega_{p1} \ll \omega_{p2}$) which results in

$$A_{f,dc} \cong \frac{G_{m1}\, G_{m2}}{G_{ds1}\,(G_{m2} + G_{ds2})} \cong \frac{G_{m1}}{G_{ds1}}, \tag{3.22}$$

$$\omega_z \cong \frac{G_{m2}}{C_{p2}}, \tag{3.23}$$

$$\omega_{p1} \cong \frac{G_{m2}}{C_L + C_{p1}\, G_{m2}/G_{ds1}}, \tag{3.24}$$

$$\omega_{p2} \cong \frac{G_{ds1}}{C_{p1} + C_{p2}} \left(1 + \frac{C_{p1}}{C_L}\, \frac{G_{m2}}{G_{ds1}}\right). \tag{3.25}$$

We can consider that ω_{p1} is the dominant pole whereas ω_{p2} is the non-dominant pole.

The parameters are calculated in Table 3.8.

Table 3.8: Estimation of the small-signal forward gain parameters.

Parameter	Value	Unit
$A_{f,dc}$	244.234	-
$A_{f,dc}$	47.756	dB
f_z	1089.51	MHz
f_{p1}	863.215	kHz
f_{p2}	3.228	MHz
f_u	26.085	MHz

We see that the dominant and non-dominant poles are actually quite close to each other since the ratio ω_{p2}/ω_{p1} is only about 3.7. The forward gain is plotted versus frequency in Figure 3.12 for the parameters given in Table 3.8.

We observe that ω_z is much higher than the unity gain frequency ω_u and that both ω_{p1} and ω_{p2} are smaller than the unity gain frequency. The unity gain frequency can therefore be approximated by

$$\omega_u \cong \sqrt{|A_{dc,ol}|\, \omega_{p1}\, \omega_{p2}} \cong \sqrt{\frac{G_{m1}\, G_{m2}}{C_L\,(C_{p1} + C_{p2})}}. \tag{3.26}$$

As shown in Figure 3.12, the unity gain frequency ω_u is actually a good estimation of the resonant frequency of the closed-loop transfer function. We also observe that the phase margin is very small $PM = 10.3\,^\circ$ leading to a strong peaking at $\omega_0 \cong \omega_u$.

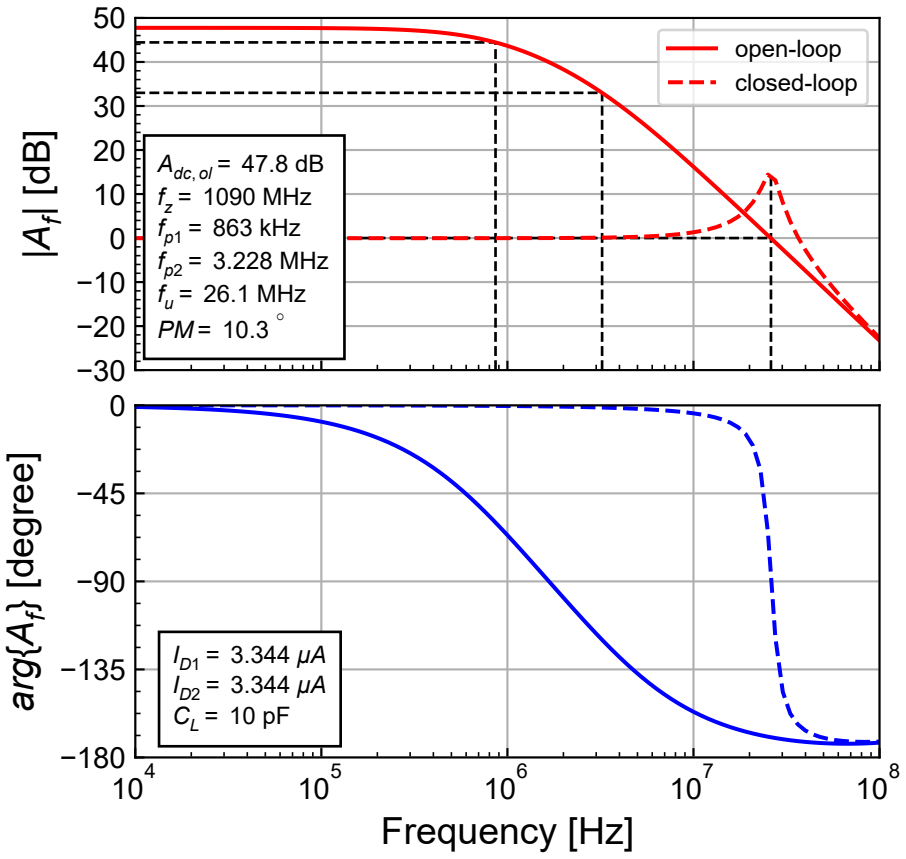


Figure 3.12: Theoretical forward gain (loop gain).

The system can be compensated by adding a compensation capacitor C_c at the drain of M_1. Assuming now that $C_c \gg C_{p2}$ we get

$$A_f(s) = L(s) \triangleq \frac{\Delta V_{out}}{\Delta V_{in}} = A_{f,dc} \frac{1 + s/\omega_z}{(1 + s/\omega_{p1})(1 + s/\omega_{p2})}. \tag{3.27}$$

The parameters can be derived assuming that $\omega_{p1} \ll \omega_{p2}$, resulting in

$$A_{f,dc} \cong \frac{G_{m1} G_{m2}}{G_{ds1}(G_{m2} + G_{ds2})} \cong \frac{G_{m1}}{G_{ds1}}, \tag{3.28}$$

$$\omega_z \cong \frac{G_{m2}}{C_c}, \tag{3.29}$$

$$\omega_{p1} \cong \frac{G_{m2}}{C_L + C_c(1 + G_{ds2}/G_{ds1}) + C_{p1} G_{m2}/G_{ds1}}, \tag{3.30}$$

$$\omega_{p2} \cong \frac{G_{ds1}}{C_c} + \frac{G_{ds1} + G_{ds2}}{C_L} + \frac{G_{m2} C_{p1}}{C_L C_c}. \tag{3.31}$$

The parameters for the circuit with compensation capacitor C_c at the drain of M_1 are given in Table 3.9. The open- and closed-loop transfer functions for these parameters are plotted in Figure 3.13.

Table 3.9: Estimation of the small-signal forward gain parameters with compensation capacitor C_c at the drain of M_1.

Parameter	Value	Unit
C_L	10	pF
C_c	10	pF

Table 3.9: Estimation of the small-signal forward gain parameters with compensation capacitor C_c at the drain of M_1.

Parameter	Value	Unit
$A_{f,dc}$	244.234	-
$A_{f,dc}$	47.756	dB
f_z	0.973	MHz
f_{p1}	283.995	kHz
f_{p2}	14.034	kHz
f_u	0.987	MHz

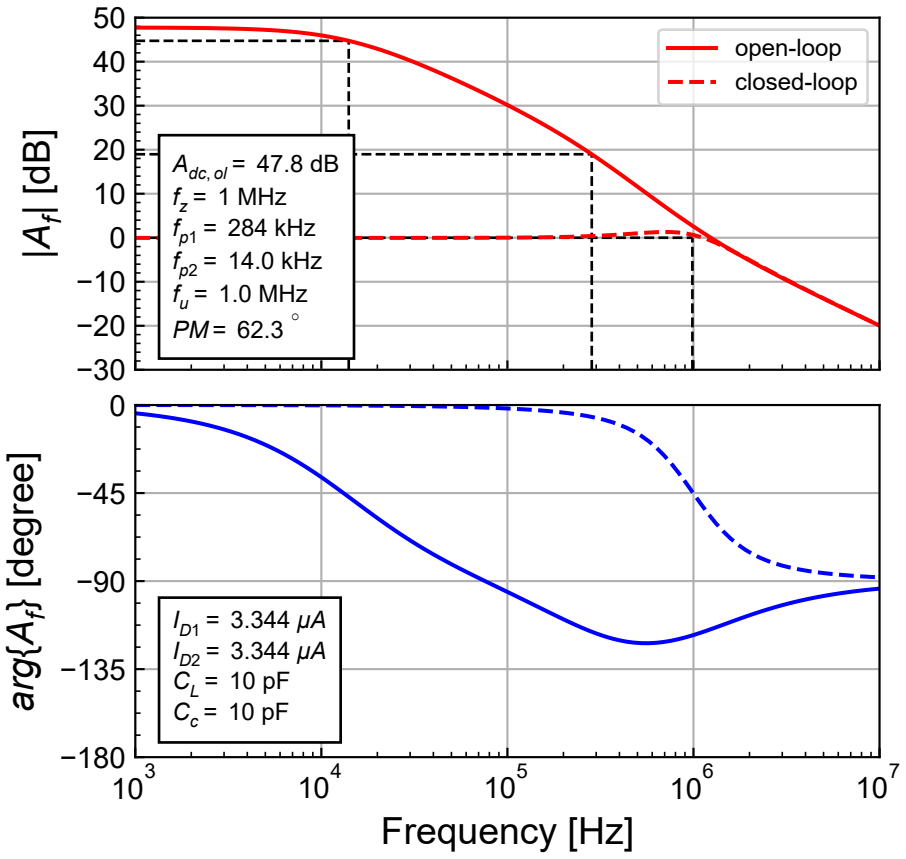


Figure 3.13: Theoretical forward gain (loop gain) and closed-loop gain with compensation capacitor C_c at the drain of M_1.

From Figure 3.13, we oberve that the phase margin has now increased to $PM = 62.3\ ^\circ$ and the peaking has almost disappeared resulting in a much better step response. On the other hand the SSF bandwidth has now decreased to that of the SVF. This mitigates the above finding that the SSF has a much larger bandwidth than the SVF. This observation was obtained without considering the parasitic capacitances and the need to compensate the circuit to obtain a reasonable step response.

The main reason to use the SSF is therefore to take adavantage of its low output resistance. We will estimate the output impedance in the next section.

3.4 Output impedance

The main reason to use the SSF instead of the SVF is its low output resistance [6]. We now will derive an expression of the SSF output impedance first without compensation capacitance using the

small-signal schematic shown in Figure 3.14.

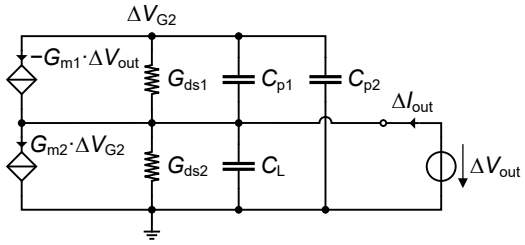


Figure 3.14: Small-signal schematic of the FVF for calculation of the output impedance.

If we assume that $C_L \gg C_{p1}, C_{p2}$, we get

$$Z_{out}(s) = R_{out} \frac{\frac{s}{\omega_z} + 1}{\left(\frac{s}{\omega_0}\right)^2 + \frac{s}{\omega_0 Q} + 1} \tag{3.32}$$

with

$$R_{out} = \frac{G_{ds1}}{G_{m1}\, G_{m2} + G_{ds1}\,(G_{m2} + G_{ds2})} \cong \frac{G_{ds1}}{G_{m1}\, G_{m2}}, \tag{3.33}$$

$$\omega_z = \frac{G_{ds1}}{C_{p1} + C_{p2}}, \tag{3.34}$$

$$\omega_0 \cong \sqrt{\frac{G_{m1}\, G_{m2}}{C_L\,(C_{p1} + C_{p2})}}, \tag{3.35}$$

$$Q \cong \frac{\sqrt{C_L\,(C_{p1} + C_{p2})\, G_{m1}\, G_{m2}}}{C_L\, G_{ds1} + C_{p2}\, G_{m1} + C_{p1}\, G_{m2}}. \tag{3.36}$$

The parameters for calculating the output impedance for the current design are given in Table 3.10.

Table 3.10: Estimation of the small-signal parameters for calculating the output impedance assuming that $C_L \gg C_{p1}, C_{p2}$.

Parameter	Value	Unit
R_{out}	66.668	Ω
$G_{m1}\, R_{out}$	0.004189	-
f_z	0.973	MHz
f_0	26.085	MHz
Q	6.772	-

From Table 3.10 we see that the output resistance $R_{out} = Z_{out}(0)$ is about 239-times smaller than that of the SVF. We can compare the theoretical expression (3.32) to ngspice simulations. The resulting output impedance normalized to that of the SVF $G_{m1}\, Z_{out}$ is compared to simulation results in Figure 3.15.

We see that the estimated output resistance $R_{out} = 66.668\ \Omega$ and $G_{m1}\, R_{out} = 4.189\text{e-}03$ are larger than the simulated values $R_{out} = 32.332\ \Omega$ and $G_{m1}\, R_{out} = 1.983\text{e-}03$. This is due to the difference between the estimated and simulated values of the transistor output conductances G_{ds1} and G_{ds2}. Indeed the simulated values of the output conductances are $G_{ds1} = 120\ nA/V$ and $G_{ds2} = 165\ nA/V$ compared to $G_{ds1} = 257\ nA/V$ and $G_{ds2} = 334\ nA/V$ for the theoretical estimations.

We have seen that to avoid the strong peaking in the closed-loop transfer function, we can add a compensation capacitor which lowers the dominant pole of the open-loop transfer function avoiding the peaking in the closed-loop transfer function. The drawback is that it significantly reduces the

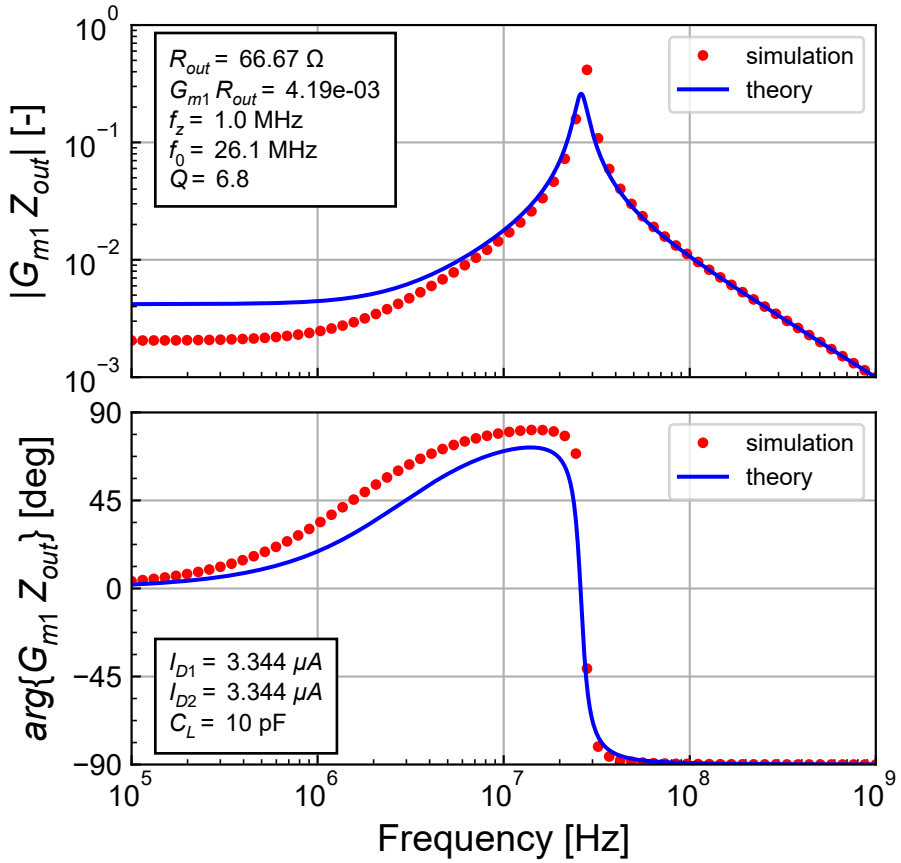


Figure 3.15: Simulated output impedance normalized to $1/G_{m1}$ and compared to the theoretical expression assuming that $C_L \gg C_{p1}, C_{p2}$.

bandwidth, canceling the advantage of the SSF compared to the SVF. How does the compensation capacitance affect the output impedance?

Let's consider the case where the compensation capacitor C_c is connected between the drain of M_1 and ground. If we assume that C_c is of the same order of magnitude than the load capacitance C_L and that $C_L, C_c \gg C_{p1}, C_{p2}$, we get the same expression for Z_{out} than in (3.32) but with the following parameters

$$R_{out} \cong \frac{G_{ds1}}{G_{m1}\, G_{m2}}, \tag{3.37}$$

$$\omega_z = \frac{G_{ds1}}{C_c}, \tag{3.38}$$

$$\omega_0 \cong \sqrt{\frac{G_{m1}\, G_{m2}}{C_L\, C_c}}, \tag{3.39}$$

$$Q \cong \sqrt{\frac{C_L}{C_c}\,\frac{G_{m1}}{G_{m2}}}. \tag{3.40}$$

The parameters are calculated in Table 3.11 and the corresponding output impedance normalized to the resistance of the SVF $1/G_{m1}$ is plotted versus frequency in Figure 3.16.

Table 3.11: Estimation of the small-signal parameters for calculating the output impedance with a compensating capacitance C_c assuming that $C_L, C_c \gg C_{p1}, C_{p2}$ and $G_{m1} \gg G_{ds1}$ and $G_{m2} \gg G_{ds2}$.

Parameter	Value	Unit
R_{out}	66.942	Ω
$G_{m1}\, R_{out}$	0.004206	-
f_z	4.092	kHz
f_0	0.988	MHz
Q	0.976	-

The low output resistance now only holds up to the frequency of the zero $f_z = 4.092\ kHz$. Above that it increases to reach the value obtained by the SVF at the resonance frequency $f_0 = 0.988\ MHz$.

3.5 Stability analysis

In the previous sections we have seen that the SSF closed-loop transfer function shows a strong peaking that might degrade the step response. The step response can be improved by adding a compensation capacitance that lowers the dominant pole at the cost of a lower bandwidth for the same current consumption.

In this Section we want to analyze the stability of the circuit by setting an appropriate DC voltage at the input, opening the loop by disconnecting the gate of M_2, applying a test signal at its gate and looking the signal that is fed back to the drain of M_1 (small-signal voltage ΔV_2) as shown in Figure 3.17.

> **Note**
>
> Note that strictly speaking, a 2nd-order system is actually always stable, because the phase only tends to 180° asymptotically. However, because of additional high frequency poles, the phase may turn more than 180° and lead to an unstable system.

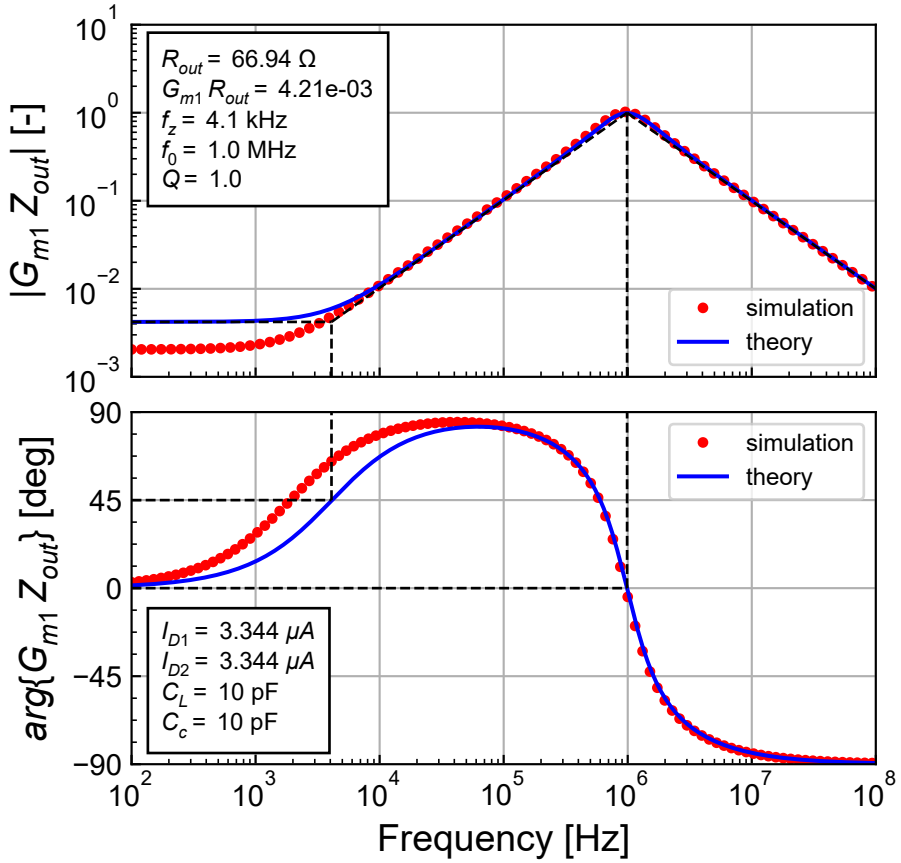


Figure 3.16: Simulated output impedance normalized to $1/G_{m1}$ and compared to the theoretical expression with a compensation capacitance $C_c = C_L$ and assuming that $C_L, C_c \gg C_{p1}, C_{p2}$ and $G_{m1} \gg G_{ds1}$ and $G_{m2} \gg G_{ds2}$.

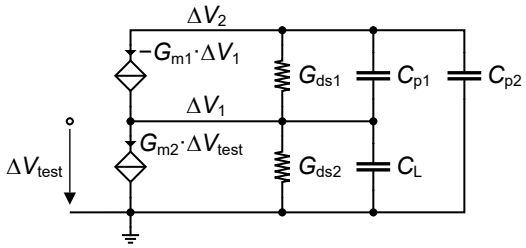


Figure 3.17: Small-signal schematic of the SSF for analyzing the stability by opening the loop at the gate of M_2.

The open-loop gain $A_{ol}(s)$ which also corresponds to the loop-gain $L(s)$ is given by

$$A_{ol}(s) = L(s) \triangleq \frac{\Delta V_2}{\Delta V_{test}} = A_{dc,ol} \frac{1 + s/\omega_z}{(1 + s/\omega_{p1})(1 + s/\omega_{p2})}. \tag{3.41}$$

The parameters can be derived assuming that the poles are sufficiently widely separated (i.e. $\omega_{p1} \ll \omega_{p2}$) which results in

$$A_{dc,ol} = -\frac{(G_{m1} + G_{ds1}) G_{m2}}{G_{ds1} G_{ds2}} \cong \frac{G_{m1} G_{m2}}{G_{ds1} G_{ds2}}, \tag{3.42}$$

$$\omega_z = \frac{G_{m1} + G_{ds1}}{C_{p1}} \cong \frac{G_{m1}}{C_{p1}}, \tag{3.43}$$

$$\omega_{p1} = \frac{G_{ds1} G_{ds2}}{C_L G_{ds1} + C_{p1} G_{ds2} + C_{p2}(G_{m1} + G_{ds1} + G_{ds2})} \cong \frac{G_{ds2}}{C_L + C_{p2} G_{m1}/G_{ds1}}, \tag{3.44}$$

$$\omega_{p2} = \frac{C_L G_{ds1} + C_{p1} G_{ds2} + C_{p2}(G_{m1} + G_{ds1} + G_{ds2})}{C_{p1} C_{p2} + C_L (C_{p1} + C_{p2})} \cong \frac{G_{ds1}}{C_{p1} + C_{p2}} \left(1 + \frac{C_{p2}}{C_L} \frac{G_{m1}}{G_{ds1}}\right). \tag{3.45}$$

We can consider that ω_{p1} is the dominant pole whereas ω_{p2} is the non-dominant pole.

The small-signal parameters are recalculated in Table 3.12.

> **Note**
>
> Note that the loop-gain given by (3.41) is different than the loop-gain given by (3.21). This is because the input and output voltages are not the same leading to different transfer functions. The feedback analysis was done more from the perspective of the input to output signal path, whereas the stability analysis only looks at the loop gain from a stability perspective without consideration on the signal path.

Table 3.12: Estimation of the small-signal parameters for the calculation of the open-loop gain.

Parameter	Value	Unit
G_{m1}	62.832	$\mu A/V$
G_{m2}	61.164	$\mu A/V$
G_{ds1}	257.261	nA/V
G_{ds2}	334.439	nA/V
G_{m1}/G_{ds1}	244.234	-
G_{m1}/G_{ds1}	47.756	dB
G_{m2}/G_{ds2}	182.885	-
G_{m2}/G_{ds2}	45.244	dB
C_{p1}	5.371	fF
C_{p2}	8.935	fF
A_{dc}	44666.7	-
A_{dc}	93	dB
f_z	1861.73	MHz
f_{p1}	4.369	kHz
f_{p2}	3.487	MHz
f_u	26.085	MHz
PM	8.425	$^\circ$

We can simulate the open-loop transfer function using the schematic shown in Figure 3.18. We need to add two transistors M_3 and M_4 to generate the DC bias voltage that needs to be applied to the gate of M_2 to have the correct bias current.

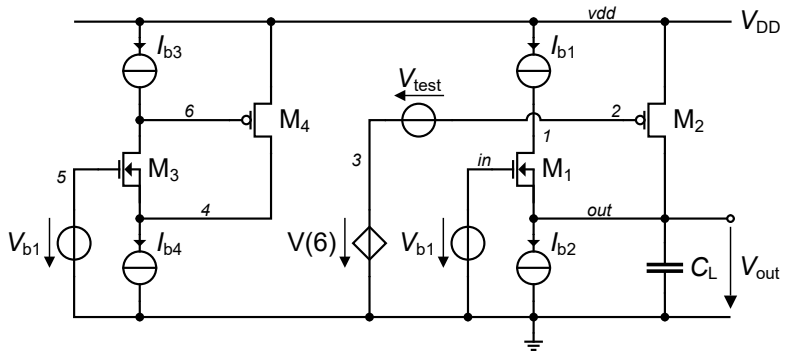


Figure 3.18: Schematic of the SSF used for the simulation of the open-loop gain.

Note that since we now have opened the loop disconnecting the gate of M_2, the parasitic capacitances associated to its gate, namely C_{GS2}, C_{GB2} and C_{GD2} no more load the drain of M_1. We therefore have to add them to the circuit to be simulated. This is why we have added in the netlist a capacitance $CGD2$ of value C_{GD2} between the drain and source of M_1 and a capacitance $CG2$ of value $C_{G2} = C_{GS2} + C_{GB2}$ between the drain of M_1 and ground.

Warning

When opening the loop in a feedback system, we always need to make sure that opening the loop does not change the impedances seen at the node where the loop is opened.

The simulation results of the open-loop gain are compared to the theoretical estimation in Figure 4.12.

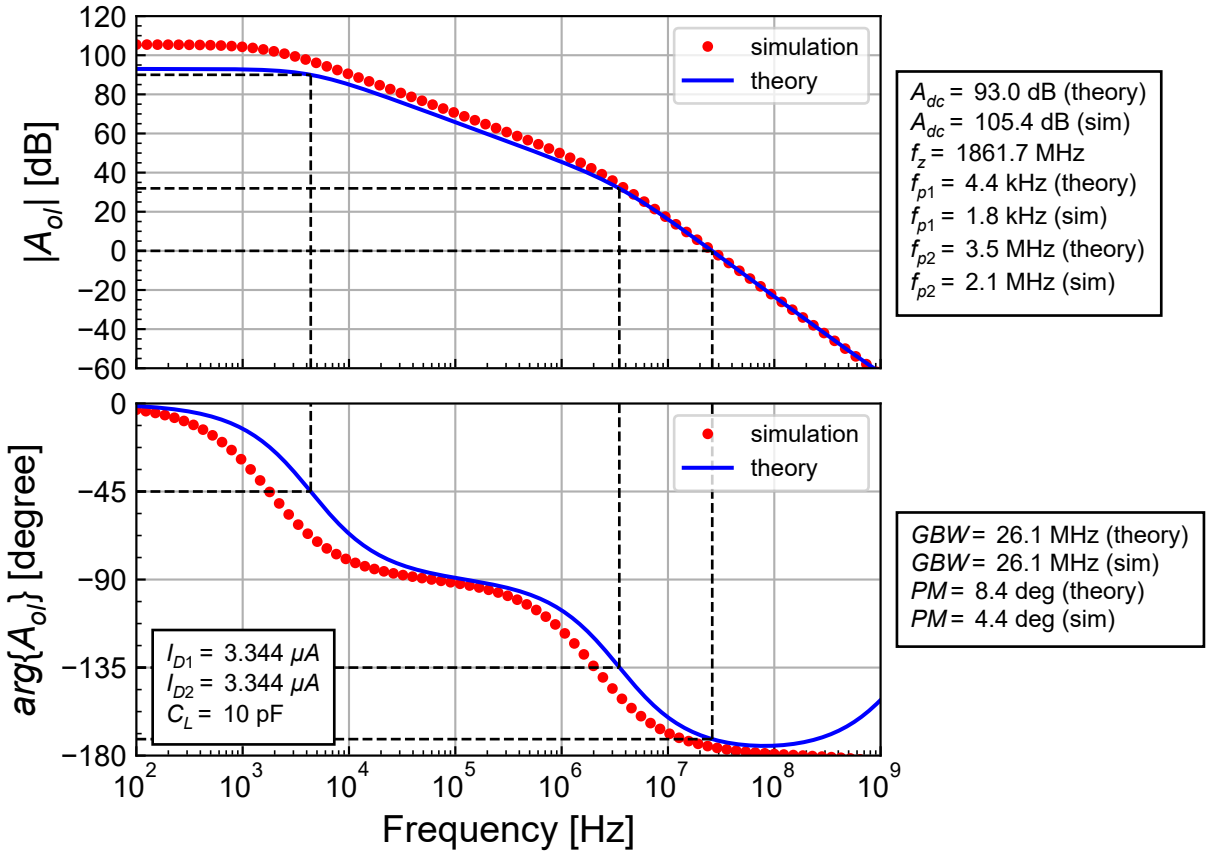


Figure 3.19: Simulated gain response compared to theoretical estimation.

We see a reasonable match between the simulation and the theoretical results. The discrepancy below

the unity gain frequency is only due to an overestimation of the transistor output conductances G_{ds1} and G_{ds2}. We can see that the circuit is actually stable but with a very small phase margin $PM = 8.4°$.

If we add a compensation capacitance C_c of the same order of magnitude than C_L in parallel to C_{p2}, then (3.41) remains unchanged but the parameters assuming that $C_{p1}, C_{p2} \ll C_L, C_c$, $G_{ds1} \ll G_{m1}$ and $G_{ds2} \ll G_{m2}$ become

$$A_{dc,ol} \cong \frac{G_{m1}\, G_{m2}}{G_{ds1}\, G_{ds2}}, \tag{3.46}$$

$$\omega_z \cong \frac{G_{m1}}{C_{p1}}, \tag{3.47}$$

$$\omega_{p1} \cong \frac{G_{ds1}\, G_{ds2}}{C_c\, G_{m1}}, \tag{3.48}$$

$$\omega_{p2} \cong \frac{G_{m1}}{C_L}. \tag{3.49}$$

Adding a compensation capacitor C_c at the drain of M_1 will reduce the dominant pole and increase the non-dominant up to G_{m1}/C_L, without affecting the zero. This is similar to the pole splitting technique that is used for compensating OPAMPs [1].

The small-signal parameters calculated for a compensation capacitance value equal to the load capacitance results in the parameters given in Table 3.13. The loop-gain for these parameters is compared to simulations in Figure 3.20.

Table 3.13: Estimation of the small-signal parameters for the calculation of the open-loop gain with compensation capacitance.

Parameter	Value	Unit
C_L	10	pF
C_c	10	pF
A_{dc}	44849.6	-
A_{dc}	93.035	dB
f_z	1869.36	MHz
f_{p1}	0.022	kHz
f_{p2}	1.012	MHz
f_u	0.988	MHz
PM	45.728	°

We see a very good match between the theoretical estimation and the simulation result except at low frequency. This is again due to the higher estimated values of the output conductances G_{ds1} and G_{ds2} compared to the simulated values. The phase margin has now increased to $PM = 52.4$ ° which will ensure an acceptable step response which still shows some overshoot as shown in Figure 3.21.

Of course adding a compensation capacitance C_c as large as the load capacitance comes at a high area cost (doubling the area considering that $C_c = C_L$).

3.6 Voltage compliance

For checking the input-output voltage compliance, we use the schematic shown in Figure 3.22 where we have replaced the ideal current sources by current mirrors M_{3a}-M_{3b} and M_{4a}-M_{4b}. In order to simulate the circuit of Figure 3.22, we need to size the current mirrors. We choose to bias them at the onset of strong inversion setting their inversion coefficient to $IC_3 = IC_4 = 10$. For $L_3 = 1.00\ \mu m$, we get $W_3 = 0.83\ \mu m$ and for $L_4 = 1.00\ \mu m$, we get $W_4 = 1.74\ \mu m$.

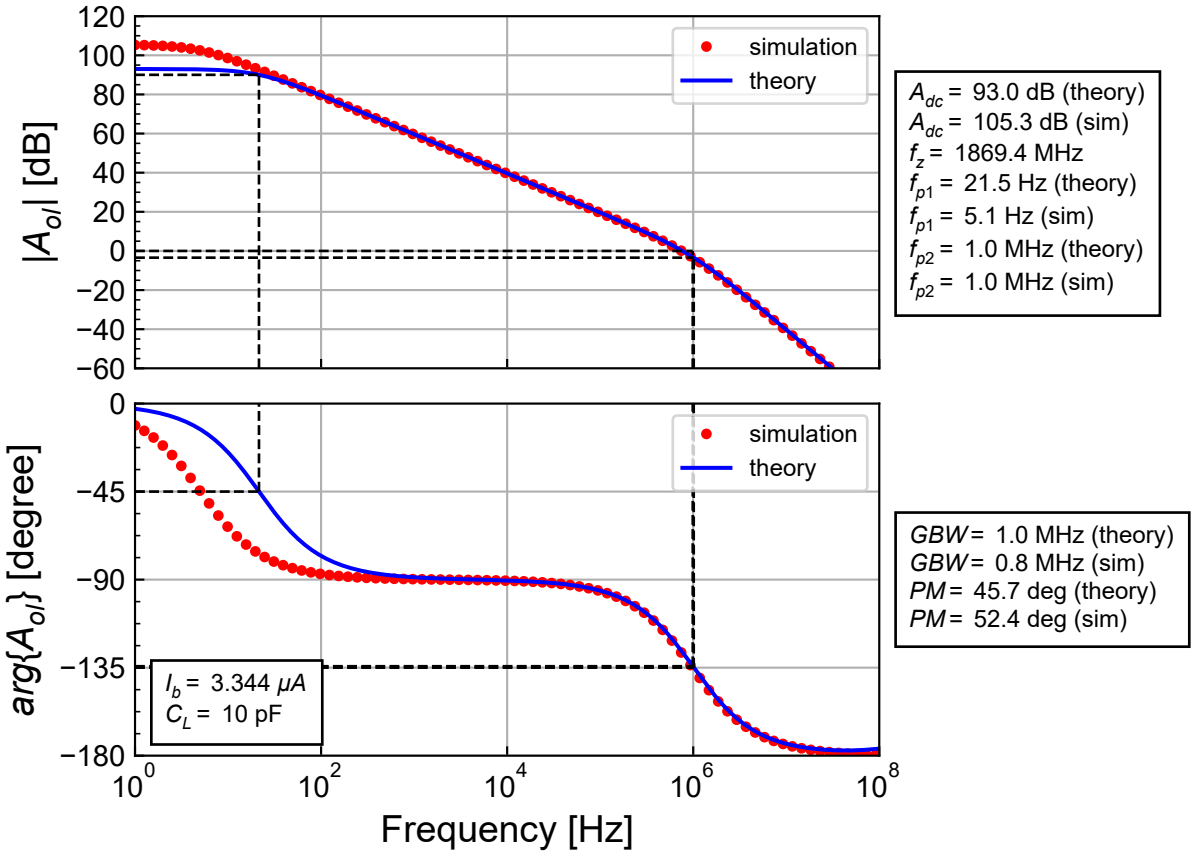


Figure 3.20: Simulated gain response compared to theoretical estimation.

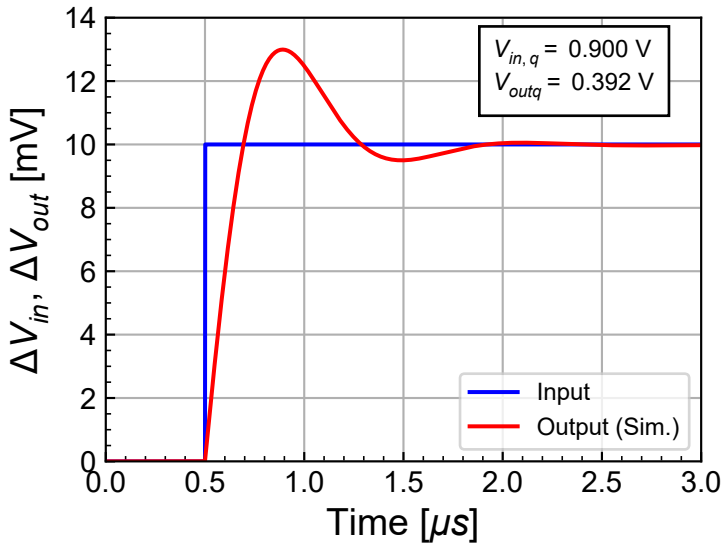


Figure 3.21: FVF step response with compensation capacitor C_c.

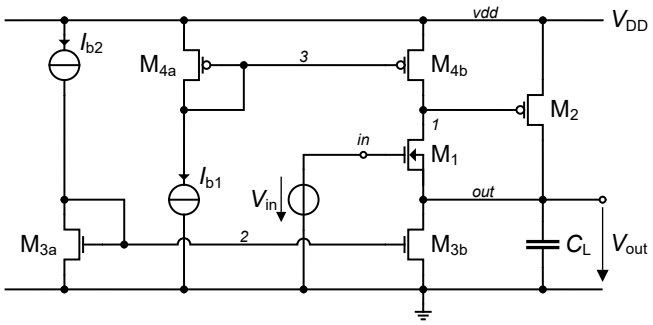


Figure 3.22: Schematic used for the DC simulation.

The minimum input voltage is defined as the voltage for which the output voltage gets equal to zero. It is approximately given by $V_{in,min} \cong V_{GS1} \cong 0.470\ V$ and the maximum input voltage is equal to $V_{in,max} \cong V_{GS1} - V_{DSsat1} + V_{BG2} + V_{DD} \cong 1.695\ V$. The SSF can therefore operate with an input voltage ranging between $0.470\ V$ and $1.695\ V$, corresponding to a wide input voltage range of about $1.224\ V$.

This can be verified by simulating the large-signal input-output characteristic which is plotted in Figure 3.23 and favorably compared to the theoretical estimation.

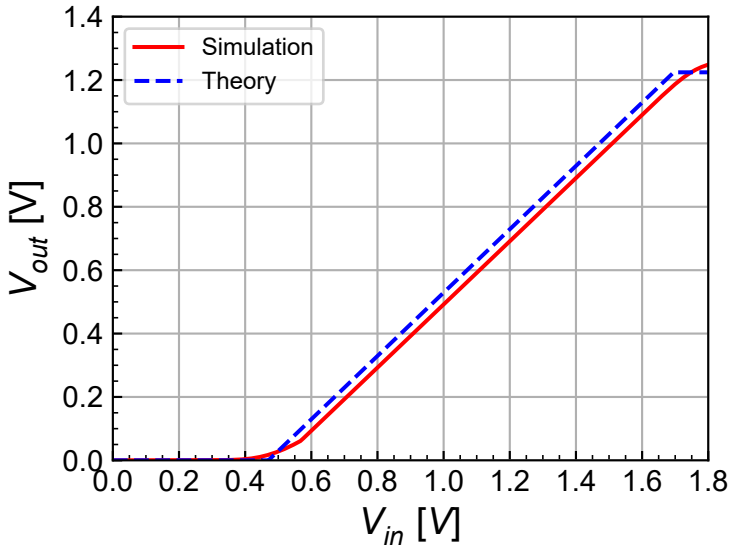


Figure 3.23: Simulated large-signal input-output characteristic.

3.7 Summary

The SSF uses a common-source stage in a feedback loop to reduce its output resistance by a factor equal to the self-gain of a transistor compared to that of the SVF. The bandwidth is increased by the same order of magnitude. However, the transfer function can show some peaking, which is undesireable for having an acceptable step response. The circuit can be compensated by adding a compensation capacitor of the same order of magnitude than the load capacitance to increase the phase margin of the open-loop transfer function and hence reduce the peaking in the closed-loop transfer function and get an acceptable step response. Adding this compensation capacitance reduces the bandwidth to about the same value obtained for the SVF, but at the cost of a higher current consumption (about double) compared to the SVF. As a conclusion, the main advantage of the SSF compared to the SVF is its very low output resistance but it doesn't really increase the bandwidth if the circuit is compensated with a compensation capacitance of the same order of magnitude than the load capacitance.

> **Note**
>
> Note that the fact that the SSF features a 2^{nd}-order transfer function has been used to build power-efficient CMOS continuous-time filters [7] [8] [9] [10]

4 The flipped voltage follower (FVF)

The main drawback of the SSF is the current consumption which is about twice that of the SVF to achieve the same bandwidth assuming that the circuit is compensated. We can actually reduce the current consumption by flipping the pMOS common-source (CS) stage into a nMOS CS which can fit below the voltage follower and share the same bias current. This results in the schematic of the *flipped voltage follower* (FVF) shown in Figure 4.1 [4] [11] [5]. It is called *flipped* because the pMOS CS of the SSF has been flipped into an nMOS CS (some say that the origin of *flipped* comes from flipping the current source of the SVF and moving it to the top [5]).

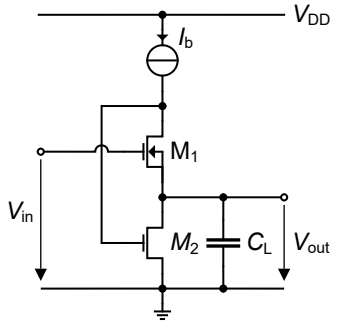


Figure 4.1: Schematic of the FVF.

Similarly to the SSF, the FVF also features a feedback loop to reduce its output resistance. The feedback loop operates as follows: if the output voltage increases keeping a constant input voltage, the drain current of M_1 decreases and the drain voltage of M_1 and gate voltage of M_2 increases. Since the gate voltage of M_2 increases its drain voltage now decreases bringing the output voltage back to its quiescent value. In other words, the FVF tries to keep the output voltage constant resulting in an output resistance that is significantly reduced compared to the SVF. We will analyze this in more details below. But before we proceed with the small-signal analysis, we need to have some large-signal considerations.

4.1 Large-signal considerations

The fact that the V_{GS} voltage of M_2 is equal to the sum of the V_{DS} voltages of M_1 and M_2 is seriously limiting the input voltage compliance. The lower limit of the input voltage corresponds to a zero output voltage and is therefore given by V_{GS1}. If we assume that M_1 is biased in moderate inversion then $V_{GS1} \cong V_{T0n}$ so the $V_{in,min} \cong V_{T0}$. This lower limit is similar to that of the SFV.

The maximum input voltage is set by transistor M_1 getting into the linear region with V_{DS} close to zero and hence $V_{in,max} \cong V_{GS1} + V_{GS2}$. If M_1 and M_2 are biased in weak or moderate inversion, $V_{in,max} \cong 2\,V_{T0}$.

The input voltage swing is therefore $\Delta V_{in} = V_{in,max} - V_{in,min} \cong V_{T0n}$ which is about one threshold voltage. For the 180 nm technology with $V_{T0n} = 0.455$, we get $V_{in,max} = 0.910\ V$, $V_{in,min} = 0.455\ V$. This leads to a very limited input voltage swing $\Delta V_{in} = 0.455\ V$.

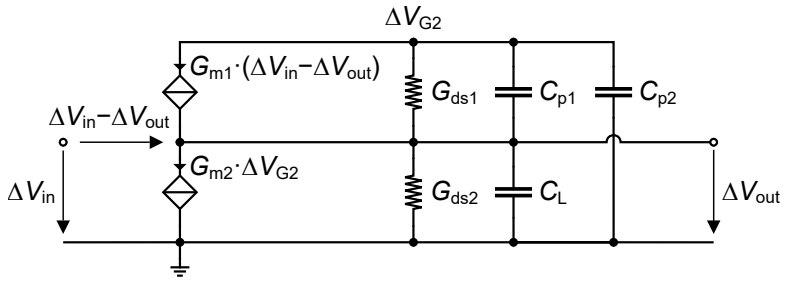


Figure 4.2: Small-signal schematic of the FVF including the parasitic capacitances C_{p1} and C_{p2}.

4.2 Small-signal analysis

The small-signal schematic of the FVF of Figure 4.1 is shown in Figure 4.2 where we have included the parasitic capacitances. Without surprise, we realize that the small-signal schematic of the FVF shown in Figure 4.2 is identical to that of the SSF shown in Figure 3.6. This means that all the small-signal derivations we have performed for the SSF are also valid for the FVF. The FVF therefore also shows a 2^{nd}-order transfer function given by (3.5) with the parameters given by (3.6), (3.7), (3.8) and (3.9). We can check this by designing the FVF for the same specifications Table 4.1 and with the same bias current I_b as used for the SVF.

Table 4.1: FVF specifications.

Specification	Symbol	Value	Unit
Minimum bandwidth	BW	1	MHz
Load capacitance	C_L	10	pF

To save voltage, we choose to bias M_1 and M_2 in moderate inversion with $IC_1 = IC_2 = 1$. For the chosen bias current $I_b = 3.344\ \mu A$ and inversion coefficient $IC_1 = 1$, we get a transconductance $G_{m1} = 62.832\ \mu A/V$. The specific current and W/L are then equal to $I_{spec1} = 3.344\ \mu A$ and $(W/L)_1 = 4.677$. We choose a long-channel transistor for M_1 with $L_1 = 1.00\ \mu m$, we get the width $W_1 = 4.28\ \mu m$.

Since M_2 shares the same bias current and has the same inversion coefficient than M_1, it has the same transconductance $G_{m2} = 62.832\ \mu A/V$, specific current $I_{spec2} = 3.344\ \mu A$ and $(W/L)_2 = 4.677$. Choosing the same length $L_2 = L_1 = 1.00\ \mu m$, we get the same width $W_2 = 4.28\ \mu m$. M_2 is hence identical to M_1. Note that M_1 and M_2 of the FVF are also identical to M_1 of the SVF.

The transistor sizing result is summarized in Table 4.2, while the small-signal parameters are given in Table 4.3.

Table 4.2: Transistor size and bias information.

Transistor	$W\ [\mu m]$	$L\ [\mu m]$	$I_D\ [\mu A]$	$I_{spec}\ [\mu A]$	IC	$V_G - V_{T0}\ [mV]$	$V_{DSsat}\ [mV]$
M1	4.28	1.00	3.344	3.344	1.0	15	116
M2	4.28	1.00	3.344	3.344	1.0	15	116

Table 4.3: Transistor small-signal and thermal noise parameters.

Transistor	$G_{spec}\ [\mu A/V]$	$G_{ms}\ [\mu A/V]$	$G_m\ [\mu A/V]$	$G_{ds}\ [nA/V]$	γ_n
M1	129.252	79.882	62.832	257.261	0.717
M2	129.252	79.882	62.832	257.261	0.717

We now will simulate the circuit shown in Figure 4.3. We have chosen the input bias voltage $V_{inq} = 0.78\ V$ so that M_1 and M_2 have about the same V_{DS} voltage. The operating voltages are given in Table 4.4.

Table 4.4: FVF node voltages.

Node	Voltage
1	0.509286

The operating point looks fine. We can now proceed with the simulation of the voltage gain with an AC simulation. The result is shown in Figure 4.4.

Figure 4.4 shows a similar behavior than the SSF shown in Figure 3.5 confirming the 2$^{\text{nd}}$-order transfer function. To compute the theoretical transfer function (3.5), we need to estimate the parasitic capacitances C_{p1} and C_{p2}. It turns out that C_{p1} and C_{p2} are identical to the one calculated for the SSF. C_{p1} is given by (3.10) and C_{p2} is given by (3.14). Of course the value of all the parasitic capacitances associated to $M_2$are slightly different because M_2 in the SSF is a pMOS transistor.

We can now compute all the small-signal parameters in order to compute the theoretical transfer function given by (3.5). They are presented in Table 4.5.

Table 4.5: Estimation of the small-signal parameters.

Parameter	Value	Unit
G_{m1}	62.832	$\mu A/V$
G_{m2}	62.832	$\mu A/V$
G_{ds1}	257.261	nA/V
G_{ds2}	257.261	nA/V
G_{m1}/G_{ds1}	244.234	-
G_{m1}/G_{ds1}	47.756	dB
G_{m2}/G_{ds2}	182.885	-
G_{m2}/G_{ds2}	45.244	dB
C_{p1}	7.966	fF
C_{p2}	20.338	fF
A_{dc}	1	-
A_{dc}	0	dB
f_z	491.693	MHz
f_0	18.797	MHz
Q	7.683	-

We see that the resonance frequency is now $f_0 = 18.797\ MHz$ and the quality factor is $Q = 7.683$, which is indeed larger than one explaining the peaking. We can now compare the simulated transfer function to (3.5) calculated with the small-signal parameters given in Table 4.5. The result is shown in Figure 4.5.

We see that the theoretical transfer given by (3.5) matches the simulaton result bvery well. It even captures the peak close to the resonance frequency. From Table 4.5, we see that the zero frequency $f_z =$ 491.693 MHz is way above the resonance frequency $f_0 = 18.797$ MHz and can therefore be neglected. This approximation with $\omega_z \to \infty$ is shown by the dashed lines in Figure 4.5.

In many applications the peaking shown in Figure 4.5 is not acceptable. The step response will oscillate as shown in Figure 4.6 and the settling time might be even longer than what is obtained by the SVF. We now will analyze the circuit using feedback theory.

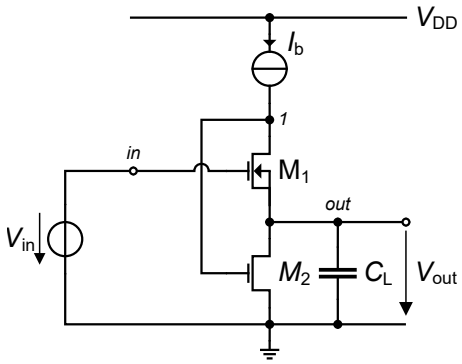


Figure 4.3: Schematic of the FVF used for simulation.

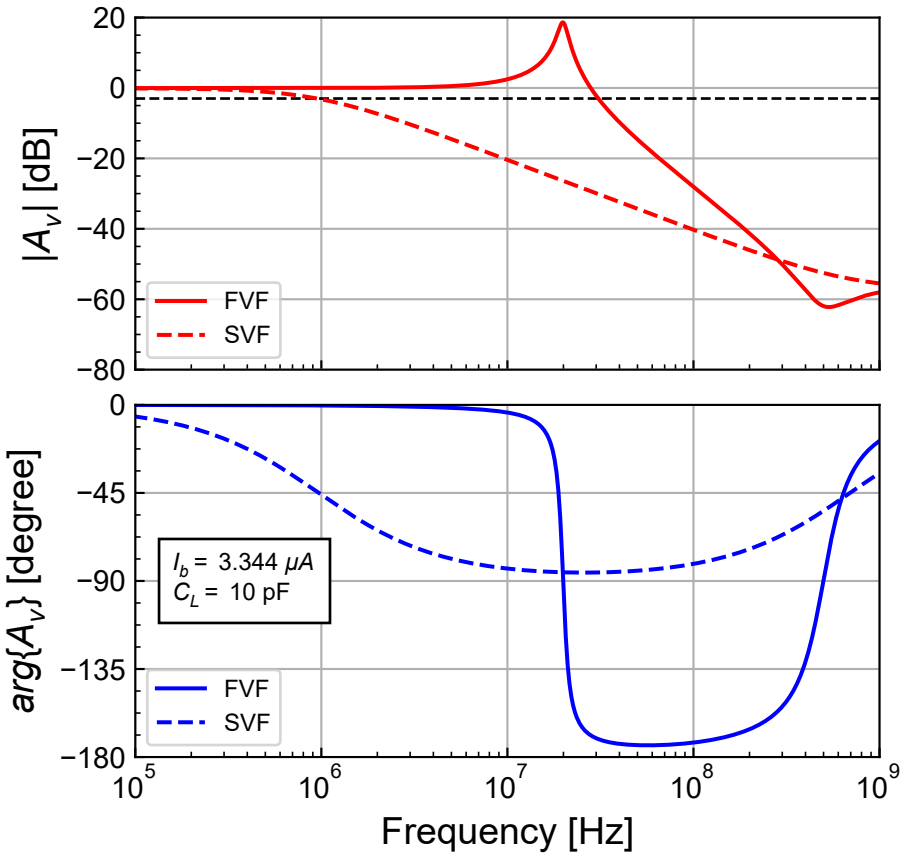


Figure 4.4: Simulated gain response compared to theoretical estimation.

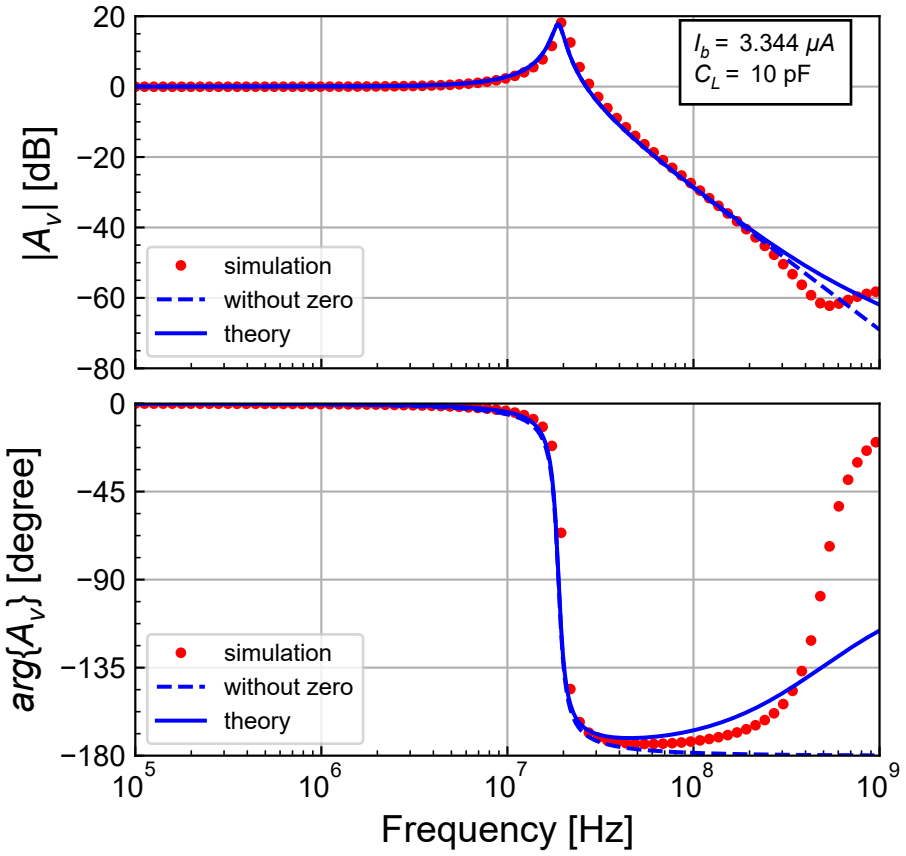


Figure 4.5: Simulated gain response compared to theoretical estimation.

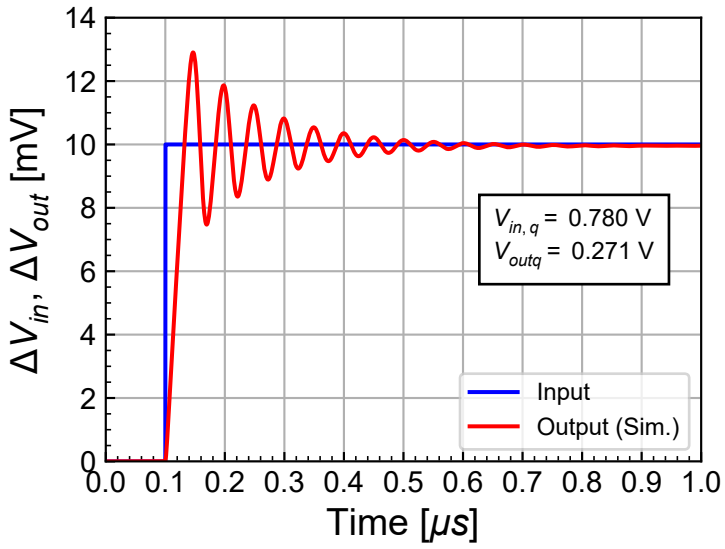


Figure 4.6: FVF step response.

4.3 Feedback analysis

We can conduct exactly the same feedback analysis for the FVF as what was done for the SSF since the small-signal circuits are identical. We then get the same foward and loop gain given by (3.21) with the parameters given by (3.22), (3.23), (3.24) and (3.25). The parameters are calculated in Table 4.6.

Table 4.6: Estimation of the small-signal forward gain parameters.

Parameter	Value	Unit
$A_{f,dc}$	244.234	-
$A_{f,dc}$	47.756	dB
f_z	491.693	MHz
f_{p1}	837.133	kHz
f_{p2}	1.728	MHz
f_u	18.797	MHz

We see that the dominant and non-dominant poles are actually quite close to each other since the ratio ω_{p2}/ω_{p1} is only about 2.1. The forward gain is plotted versus frequency in Figure 4.7 for the parameters given in Table 4.6.

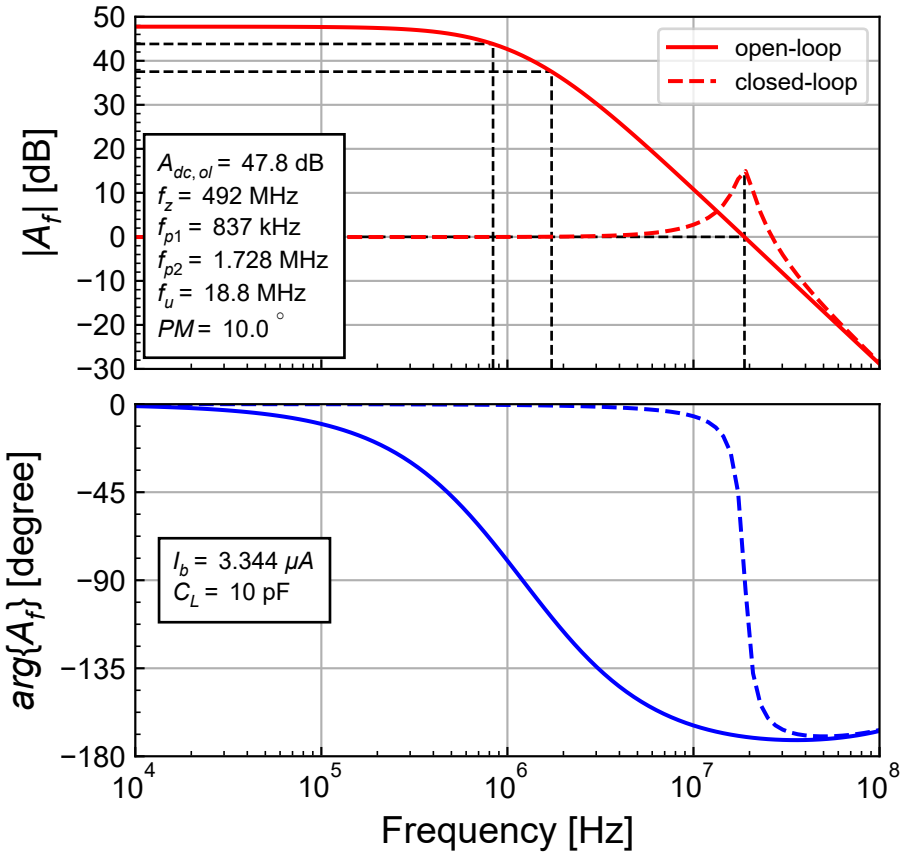


Figure 4.7: Theoretical forward gain (loop gain).

Similarly to the SSF, we observe that the ω_z is much higher than the unity gain frequency ω_u and that both ω_{p1} and ω_{p2} are smaller than the unity gain frequency. The unity gain frequency can therefore be approximated by

$$\omega_u \cong \sqrt{|A_{dc,ol}|\,\omega_{p1}\,\omega_{p2}} \cong \sqrt{\frac{G_{m1}\,G_{m2}}{C_L\,(C_{p1}+C_{p2})}}. \tag{4.1}$$

As shown in Figure 4.7, the unity gain frequency ω_u is actually a good estimation of the resonant frequency of the closed-loop transfer function. We also observe that the phase margin is very small $PM = 10.0\ ^\circ$ leading to a strong peaking at $\omega_0 \cong \omega_u$.

The system can also be compensated by adding a compensation capacitor C_c at the drain of M_1. Assuming now that $C_c \gg C_{p2}$ we get (3.27) with the parameters given by (3.28), (3.29), (3.30) and (3.31). The parameters for the circuit with compensation capacitor C_c at the drain of M_1 are given in Table 4.7. The open- and closed-loop transfer functions for these parameters are plotted in Figure 4.8.

Table 4.7: Estimation of the small-signal forward gain parameters with compensation capacitor C_c at the drain of M_1.

Parameter	Value	Unit
C_L	10	pF
C_c	10	pF
$A_{f,dc}$	244.234	-
$A_{f,dc}$	47.756	dB
f_z	1	MHz
f_{p1}	333.333	kHz
f_{p2}	13.08	kHz
f_u	1.032	MHz

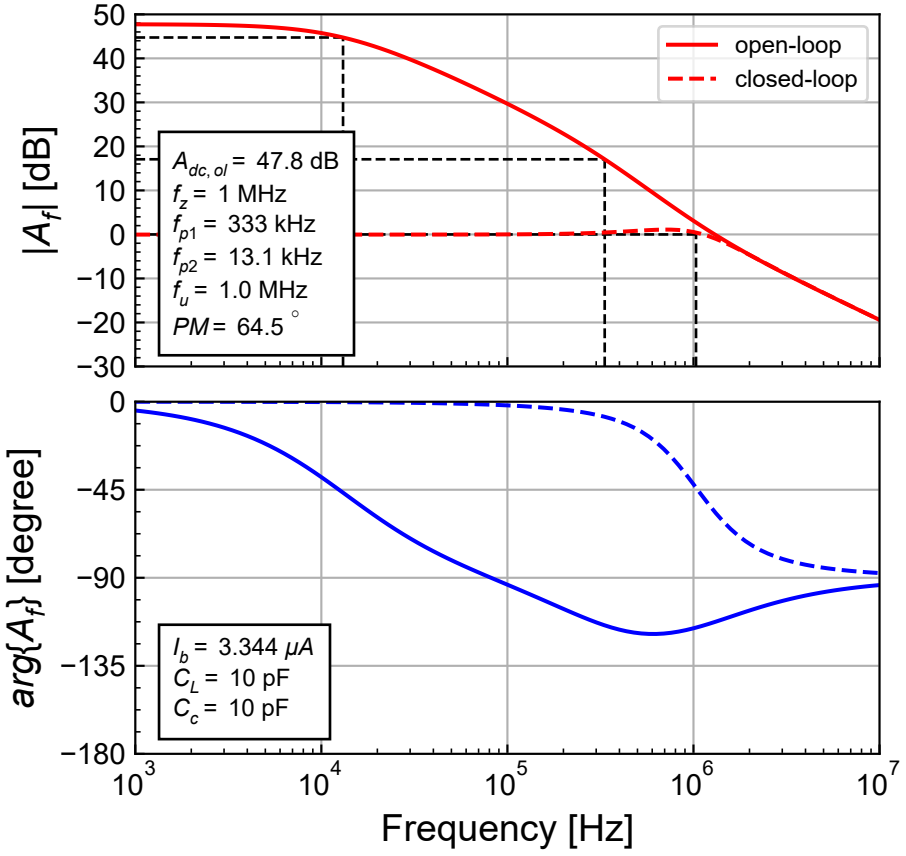


Figure 4.8: Theoretical forward gain (loop gain) and closed-loop gain with compensation capacitor C_c at the drain of M_1.

The phase margin has now increased to $PM = 64.5\ ^\circ$ and the peaking has almost disappeared resulting in a much better step response. On the other hand the FVF bandwidth has now decreased to that of the SVF.

The main reason to use the FVF is to take adavantage of its low output impedance. We will estimate the output impedance in the next section.

4.4 Output impedance

The main reason to use the FVF instead of the SVF is the low output impedance of the FVF compared to the SVF [6]. Since the small-signal circuit of the FVF is identical to that of the SSF, we can reuse the expression (3.32) found for the SSF, with the parameters given by (3.33), (3.34), (3.35) and (3.36). The parameters for calculating the output impedance for the current design are given in Table 4.8.

Table 4.8: Estimation of the small-signal parameters for calculating the output impedance assuming that $C_L \gg C_{p1}, C_{p2}$ and $G_{m1} \gg G_{ds1}$ and $G_{m2} \gg G_{ds2}$.

Parameter	Value	Unit
R_{out}	65.165	Ω
$G_{m1}\,R_{out}$	0.004094	-
f_z	1	MHz
f_0	18.797	MHz
Q	7.683	-

From Table 4.8 we see that the output resistance $R_{out} = Z_{out}(0)$ is about 244-times smaller than that of the SVF. We can compare the theoretical expression (3.32) to ngspice simulations. The resulting output impedance normalized to that of the SVF $G_{m1}\,Z_{out}$ is compared to simulation results in Figure 4.9.

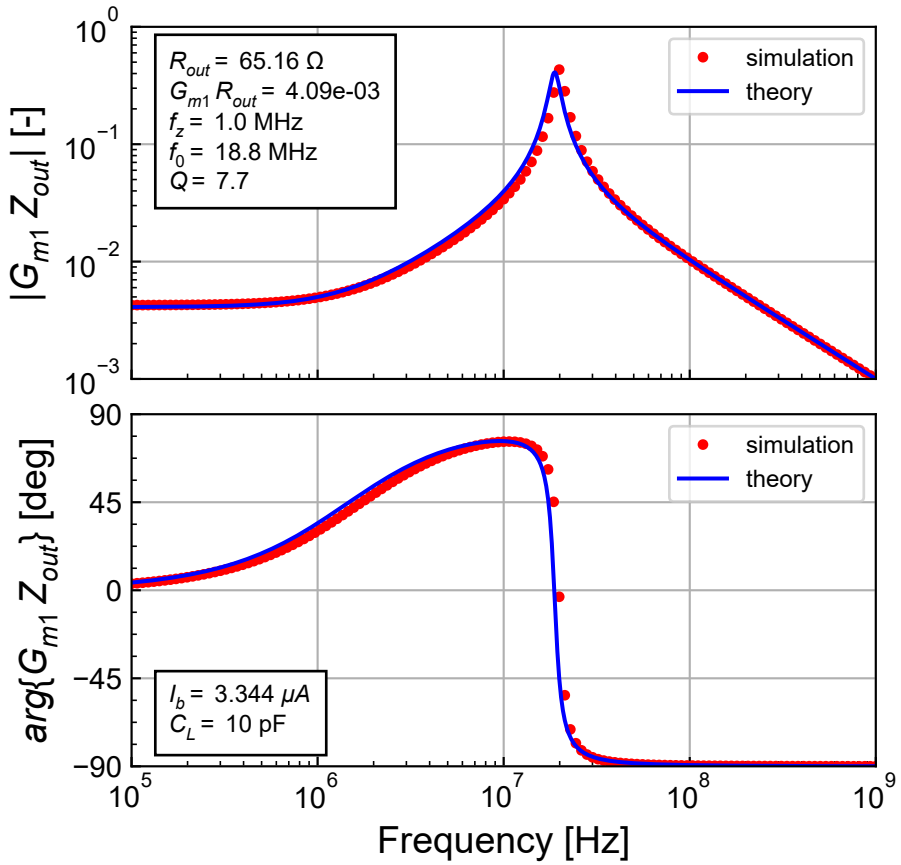


Figure 4.9: Simulated output impedance normalized to $1/G_{m1}$ and compared to the theoretical expression assuming that $C_L \gg C_{p1}, C_{p2}$.

We see an almost perfect match between the theoretical expression and the simulation. Figure 4.9 shows a very low output resistance at low frequency. However the impedance then increases and peaks to a value that gets close to that of the SVF at $f_0 = 18.797$ MHz, before decreasing.

We have seen that to avoid the strong peaking in the closed-loop transfer function, we can add a compensation capacitor which lowers the dominant pole of the open-loop transfer function avoiding the peaking in the closed-loop transfer function. The drawback is that it significantly reduces the bandwidth, canceling the advantage of the FVF compared to the SVF for the same current consumption. How does the compensation capacitance affect the output impedance?

Let's consider the case where the compensation capacitor C_c is connected between the drain of M_1 and ground. If we assume that C_c is of the same order of magnitude than the load capacitance C_L and that $C_L, C_c \gg C_{p1}, C_{p2}$, we get the same expresion (3.32) with parameters given by (3.37), (3.38), (3.39) and (3.40).

Table 4.9: Estimation of the small-signal parameters for calculating the output impedance with a compensating capacitance C_c assuming that $C_L, C_c \gg C_{p1}, C_{p2}$ and $G_{m1} \gg G_{ds1}$ and $G_{m2} \gg G_{ds2}$.

Parameter	Value	Unit
R_{out}	65.165	Ω
$G_{m1}\, R_{out}$	0.004094	-
f_z	4.094	kHz
f_0	1	MHz
Q	1	-

The low output resistance now only holds up to the frequency of the zero $f_z = 4.094\ kHz$. Above that it increases to reach the value obtained by the SVF at the resonance frequency $f_0 = 1.000\ MHz$.

4.5 Stability analysis

In the previous sections we have seen that the FVF closed-loop transfer function shows a strong peaking that might degrade the step response. The step response can be improved by adding a compensation capacitance that lowers the dominant pole at the cost of a lower bandwidth for the same current consumption.

In this Section we want to analyze the stability of the circuit in the same way it is done in [4]. The advantage is that this approach allows for the verification of the loop-gain by simulation which was not possible with the previous approach. Remember that the feedback is made of the transconductance of M_1 cascaded with the CS stage M_2. The stability can be analyzed by setting an appropriate DC voltage at the input, opening the loop by disconnecting the gate of M_2, applying a test signal at its gate and looking the signal that is fed back to the drain of M_1 (small-signal voltage ΔV_2) as shown in Figure 3.17 [4].

Similarly to the SSF, when we open the loop by discconecting the gate of M_2, the parasitic capacitances associated to its gate don't load the drain of M_1anymore. We therefore have to add these gate capacitances to the circuit netlist.

The parameters are calculated for the FVF in Table 4.10.

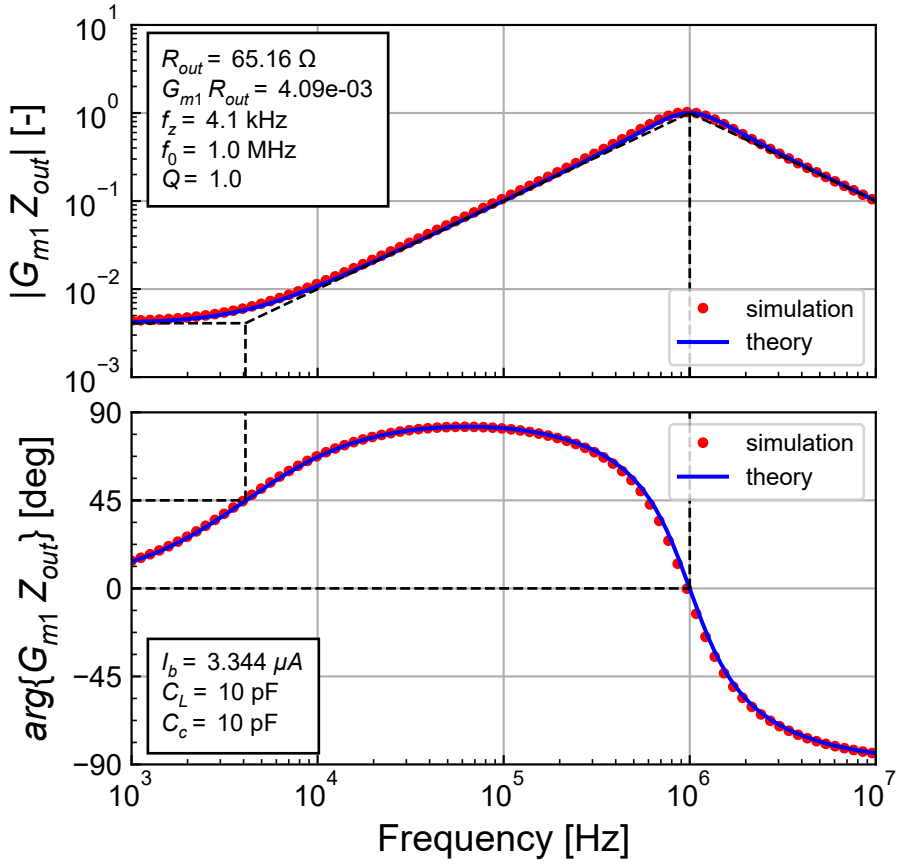


Figure 4.10: Simulated output impedance normalized to $1/G_{m1}$ and compared to the theoretical expression with a compensation capacitance $C_c = C_L$ and assuming that $C_L, C_c \gg C_{p1}, C_{p2}$ and $G_{m1} \gg G_{ds1}$ and $G_{m2} \gg G_{ds2}$.

Table 4.10: Estimation of the small-signal parameters for the calculation of the open-loop gain.

Parameter	Value	Unit
A_{dc}	59894.7	-
A_{dc}	95.548	dB
f_z	1569.85	MHz
f_{p1}	3.94	kHz
f_{p2}	5.341	MHz
f_u	35.501	MHz
PM	9.858	°

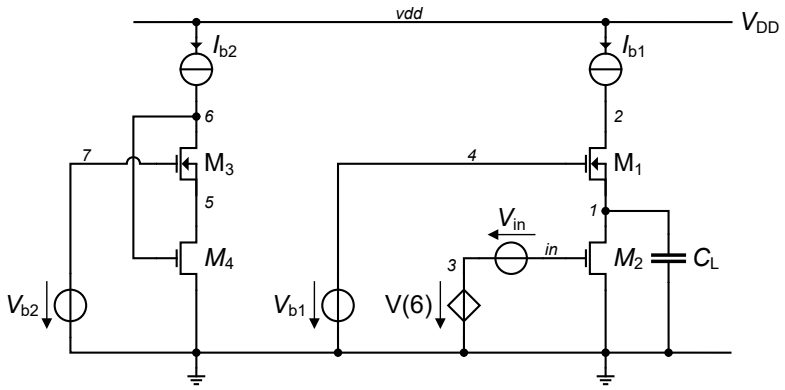


Figure 4.11: Schematic of the FVF used for the simulation of the open-loop gain.

We can simulate the open-loop transfer function using the schematic shown in Figure 4.11. We need to add M_3 and M_4 which are identical to M_1 and M_2, respectively, in order to generate the DC voltage that needs to be applied to the gate of M_2 so that its current is equal to I_b. The simulation results of the open-loop gain are compared to the theoretical estimation in Figure 4.12.

We see a reasonable match between the simulation and the theoretical results. The simulated and calculated DC gain and dominant pole are close. However, there is a small discrepancy at higher frequency with a simulated non-dominant pole $f_{p2} = 3.758\ MHz$ compared to $5.341\ MHz$.

We can see that the circuit is actually stable but with a small phase margin.

Adding a compensation capacitor C_c at the drain of M_1 with a value equal to the load capacitance results in the small-signal parameters given in Table 4.11. The loop-gain for these parameters is compared to simulations in Figure 4.13.

Table 4.11: Estimation of the small-signal parameters for the calculation of the open-loop gain with compensation capacitance.

Parameter	Value	Unit
C_L	10	pF
C_c	10	pF
A_{dc}	59894.7	-
A_{dc}	95.548	dB
f_z	1569.85	MHz
f_{p1}	0.017	kHz
f_{p2}	1.011	MHz
f_u	1.001	MHz
PM	45.31	°

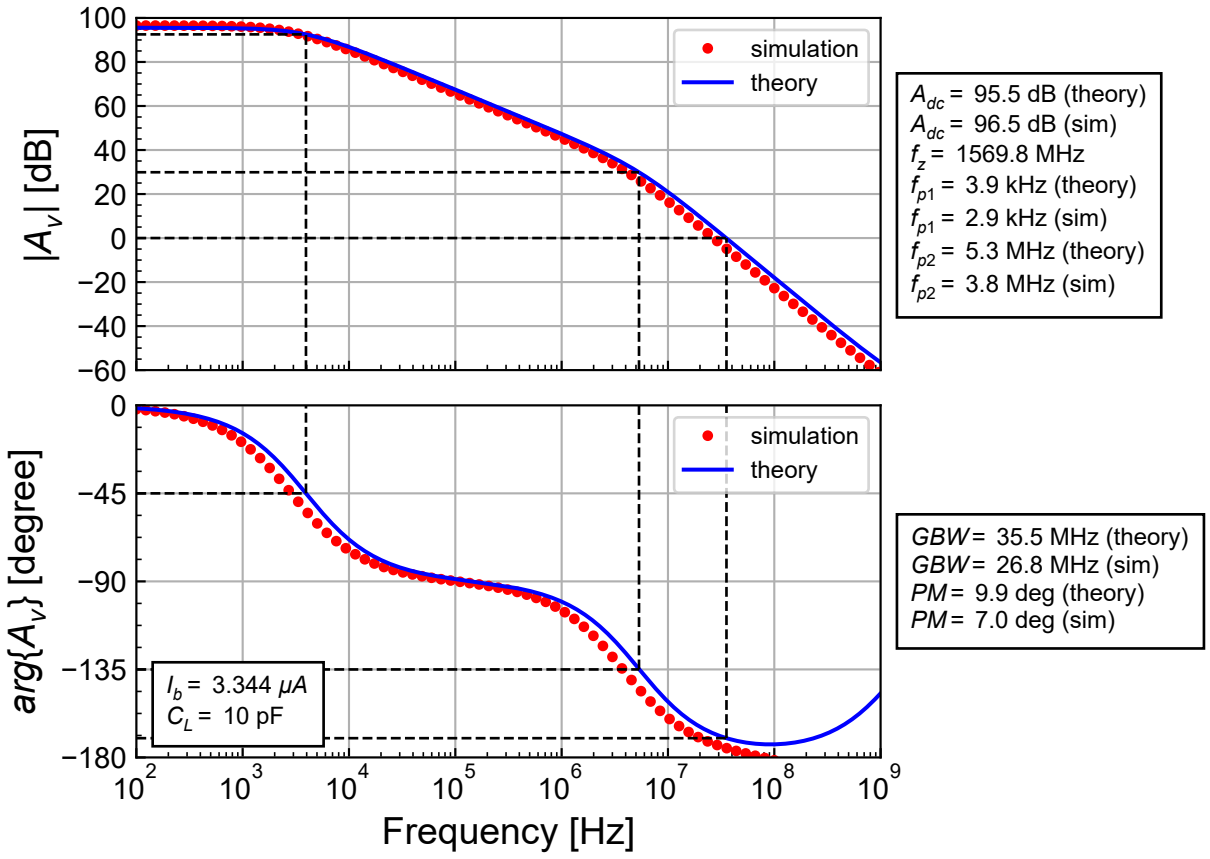


Figure 4.12: Simulated open-loop transfer function compared to theoretical estimation.

We now see a perfect match between simulation and the theoretical estimation of the open-loop transfer function with a compensation capacitor C_c connected at the drain of M_1. The dominant pole has been shifted to very low frequency and the phase margin has been increased to $PM = 52.1\ ^\circ$ which will ensure an acceptable step response which still shows some overshoot as shown in Figure 4.14.

4.6 Voltage compliance

For checking the input-output voltage compliance, we use the schematic shown in Figure 4.15 where we have replaced the ideal current source by a pMOS current mirror M_{3a}-M_{3b}.

In order to simulate the circuit of Figure 4.15, we need to size the current mirror. We choose to bias them at the onset of strong inversion setting their inversion coefficient to $IC_3 = 10$. For $L_3 = 1.00\ \mu m$, we get $W_3 = 3.53\ \mu m$.

The minimum input voltage is defined as the voltage for which the output voltage gets equal to zero. It is approximately given by $V_{in,min} \cong V_{GS1} \cong 0.470\ V$ and the maximum input voltage is equal to $V_{in,max} \cong V_{GS1} + V_{GS2} \cong 0.941\ V$. The FVF can therefore operate with an input voltage ranging between $0.470\ V$ and $0.941\ V$, corresponding to an input voltage range of about one threshol voltage $0.470\ V$. This is clearly the main drawback of the FVF.

This can be verified by simulating the large-signal input-output characteristic which is plotted in Figure 4.16 and compared to the theoretical estimation. The simulated input voltage range is about equal to the theoretical estimation

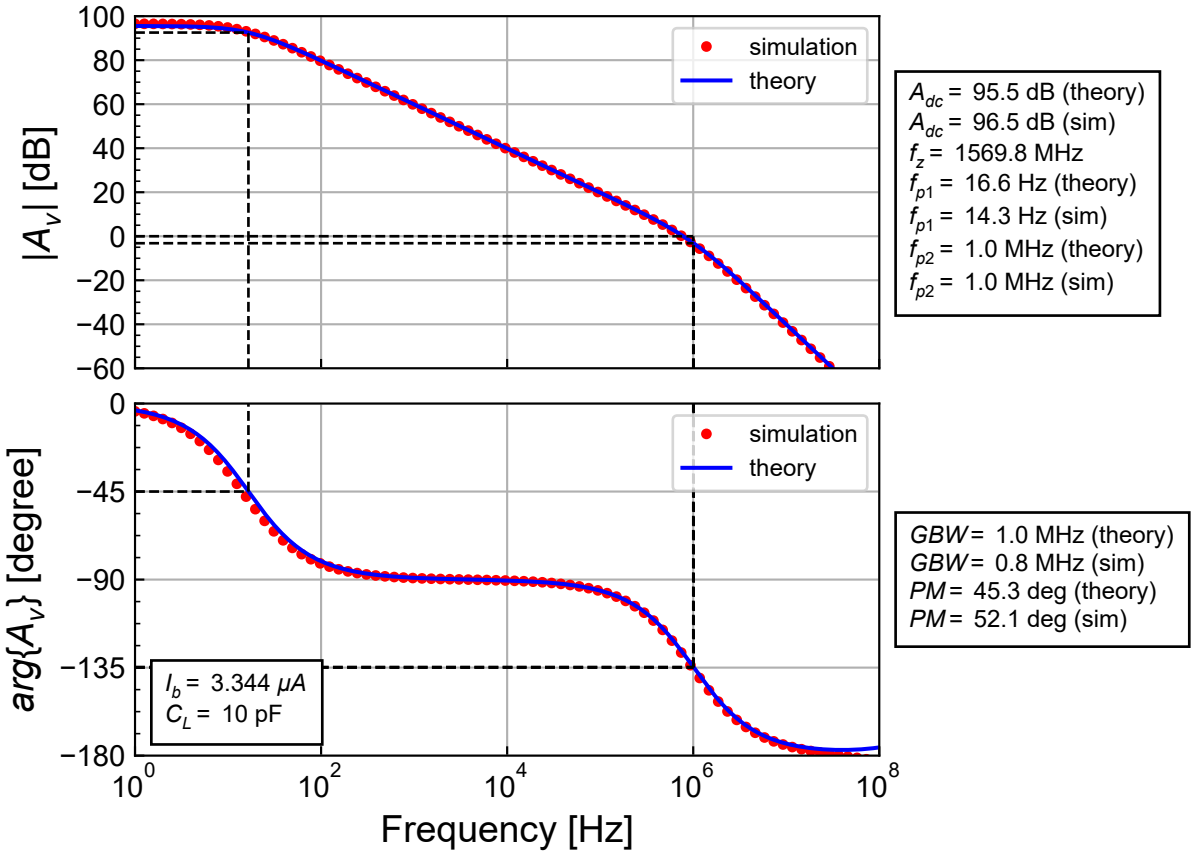


Figure 4.13: Simulated open-loop transfer function with compensation capacitor C_c compared to theoretical estimation.

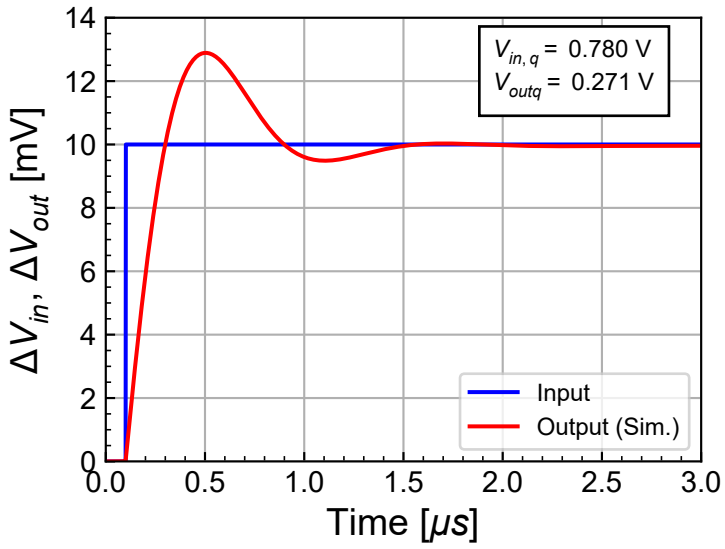


Figure 4.14: FVF step response with compensation capacitor C_c.

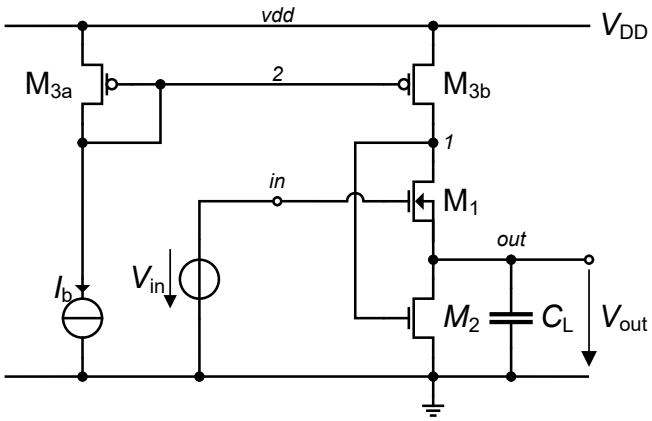


Figure 4.15: Schematic used for the DC simulation.

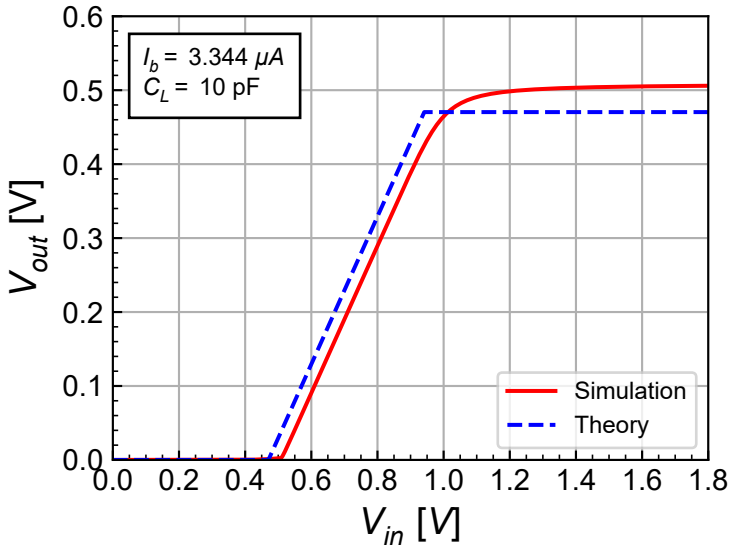


Figure 4.16: Simulated large-signal input-output characteristic.

4.7 Summary

The CS pMOS transistor of the SSF can be replaced by an nMOS CS that is stacked with M_1 resulting in the FVF. The small-signal circuit of the FVF is identical to that of the SSF and therefore the two circuit share the same results. However, because the CS stage shares the same current than the voltage follower M_1, the FVF consumes half the current compared to the SSF.

5 Conclusion

We started to analyze the simple voltage (SVF) first, showing that to have a voltage gain as close to unity requires the common-drain transistor to be in a separate well [2]. We then have evaluated the transfer function and output impedance showing that the output resistance is simply equal to $1/G_m$ of the common-drain transistor [2]. To reduce this output resistance we then have investigated two improved voltage followers, namely the super source follower (SSF) [1] [3] and the flipped voltage follower (FVF) [4] [5].

The SSF adds a common-source stage in a loop that maintains the output voltage constant resulting in a much lower output resistance [3]. Because of the feedback loop, the SSF shows a 2^{nd}-order transfer function with a high peaking at high frequency due to the parasitic capacitances at the gate of the CS transistor. We have analyzed the open-loop transfer function and found out that the circuit can be compensated similarly to a two-stage OPAMP by adding a compensation capacitor. Adding this compensation capacitor, increases the phase margin, resulting in an acceptable step response. We then looked at the output impedance which shows a low frequency output resistance that is significantly lower than that of the SVF. Adding the compensation capacitor limits the bandwidth over which the output impedance is low. The dawback of the SSF is that we need about twice the current of the SVF to achieve about the same bandwidth. The main advantage is the very low output resistance.

The FVF is derived from the SSF by replacing the pMOS CS transistor of the SSF by an nMOS which can be stacked below the voltage follower and shares the same current [4] [5] [6]. The small-signal circuit of the FVF is identical to that of the SSF and therefore all the results obtained for the SSF are also valid for the FVF. The main difference is that the FVF achieves about the same perfomance than the SSF but at half the current. It basically consumes the same current than the SVF but offers much lower output resistance. On the other hand, its input voltage compliance is rather limited compared to the SSF and SVF.

Voltage followers are key circuits that provide a unity voltage gain with a low output resistance. The SVF can be improved by using either the SSF or with the same current consumption the FVF.

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