Short-channel MOSFET Thermal Noise Modeling

Using the inversion coefficient (Version 1)

Christian Enz (christian.enz@epfl.ch)

20.06.2026

This notebook presents a model of the white noise generated by the MOS transistor that is valid in all regions of operation, from weak to strong inversion. It also describes an empirical model that accounts for the increase of the white noise due to short-channel effects.

Table of contents

Licensing **4**

1 Introduction **5**

2 Channel thermal noise conductance **6**
2.1 Long-channel (without VS) 6
2.2 Short-channel (with VS) 8

3 Thermal noise parameter δ_n **9**
3.1 Definition 9
3.2 Long-channel (without VS) 10
3.3 Short-channel (with VS) 10

4 Thermal noise excess factor γ_n **12**
4.1 Definition 12
4.2 Long-channel (without VS) 12
4.3 Short-channel (with VS) 13
4.4 Strong inversion approximation 15
4.5 Weak inversion approximation 15
4.6 Approximation valid from weak to strong inversion 15

5 Comparison with measurements **17**

6 Application to LNA design **19**
6.1 Input-referred thermal noise resistance 19
6.2 Minimum noise figure 20

7 Conclusion **22**

References **23**

Licensing

1 Introduction

Noise is important for analog IC design because it represents the fundamental lower limit for signal detection. At lower frequency, the flicker noise is dominant, particularly for advanced CMOS technologies. However, flicker noise can be reduced or even eliminated by circuit techniques such as autozero or chopper stabilization [1]. The remaining white noise then becomes the dominant noise. This white noise is mostly contributed by the MOS transistors. In this notebook we will model the white noise generated by the MOS transistor in all regions of operation, from weak to strong inversion. We also will develop a model that accounts for the increase of the white noise due to short-channel effects.

2 Channel thermal noise conductance

2.1 Long-channel (without VS)

The PSD of the drain current fluctuations due to thermal noise in the whole channel is obtained by integrating along the channel resulting in [2]

$$S_{\Delta I_D^2} = 4kT \cdot G_n, \tag{2.1}$$

where G_n is the *thermal noise conductance* at the drain which is given by [3] [2]

$$G_n = \frac{1}{L^2} \cdot \int_0^L W \cdot \mu \cdot (-Q_i(x)) \cdot dx = \mu \cdot \frac{W}{L^2} \cdot \int_0^L -Q_i(x) \cdot dx = \frac{\mu}{L^2} \cdot |Q_I|, \tag{2.2}$$

where it has been assumed that mobility is constant along the channel. We see that the thermal noise PSD and conductance at the drain is proportional to the total mobile (or inversion) charge stored in the channel

$$Q_I = W \cdot \int_0^L -Q_i(x) \cdot dx. \tag{2.3}$$

Note that the above result only holds for a long-channel transistor. In the case of a short-channel device, the assumption of constant mobility does not hold anymore and a different approach is needed [4]. This will be discussed in more details below.

At low-frequency, the drain current fluctuations due to the thermal noise generated in the channel can therefore be modelled by a noiseless transistor and a noise current source connected between the drain and source of the transistor as illustrated in Figure 2.1.

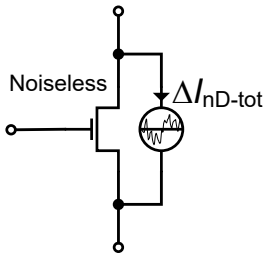

Figure 2.1: Thermal noise modeled as a noisy current source between source and drain.

Of course the thermal noise conductance G_n depends on bias. To evaluate this bias dependence, we start by normalizing G_n to G_{spec} to evaluate it in terms of the normalized source and drain charges q_s and q_d using the charge-based model

$$g_n \triangleq \frac{G_n}{G_{spec}} = \int_0^1 q_i(\xi) \cdot d\xi = q_I, \tag{2.4}$$

where

$$G_{spec} \triangleq \frac{I_{spec}}{U_T} \tag{2.5}$$

with

$$I_{spec} \triangleq I_{spec\square} \cdot \frac{W}{L} \tag{2.6}$$

and where $I_{spec\square} \triangleq 2\,n\,\mu\,C_{ox}$ is an sEKV parameter [5] [6].

The charge-based drain current expression is given by [2]

$$i_d \triangleq \frac{I_D}{I_{spec}} = -(2q_i + 1) \cdot \frac{dq_i}{d\xi}, \tag{2.7}$$

where $q_i \triangleq Q_i/Q_{spec}$ is the inversion charge Q_i normalized to $Q_{spec} \triangleq -2nU_T\,C_{ox}$ and $\xi \triangleq x/L$ the distance along the channel normalized to the channel length L [2]. We can now express ξ in terms of the drain current according to

$$d\xi = -\frac{2q_i + 1}{i_d} \cdot dq_i \tag{2.8}$$

in order to perform the integration in the charge domain [2]

$$g_n = q_I = -\frac{1}{i_d} \cdot \int_{q_s}^{q_d} q_i \cdot (2q_i + 1) \cdot dq_i = \frac{1}{i_d} \cdot \int_{q_d}^{q_s} q_i \cdot (2q_i + 1) \cdot dq_i \tag{2.9}$$

$$= \frac{1}{i_d} \cdot \frac{4q_s^3 + 3q_s^2 - 3q_d^2 - 4q_d^3}{6} \tag{2.10}$$

$$= \frac{1}{i_d} \cdot \frac{(q_s - q_d)(4q_s^2 + 3q_s + 4q_sq_d + 3q_d + 4q_d^2)}{6}. \tag{2.11}$$

The normalized charge densities at the source q_s and at the drain q_d are defined as [2]

$$q_s \triangleq q_i(\xi = 0) = \frac{Q_i(x = 0)}{Q_{spec}}, \tag{2.12}$$

$$q_d \triangleq q_i(\xi = 1) = \frac{Q_i(x = L)}{Q_{spec}}. \tag{2.13}$$

For a long-channel transistor, the normalized drain current is obtained by integrating (2.7) in the charge domain resulting in [2]

$$i_d = q_s^2 - q_d^2 + q_s - q_d = (q_s - q_d)(q_s + q_d + 1). \tag{2.14}$$

Replacing i_d from (2.14) in (2.11) and simplifying results in

$$g_n = \frac{1}{6} \cdot \frac{4q_s^2 + 3q_s + 4q_sq_d + 3q_d + 4q_d^2}{q_s + q_d + 1}. \tag{2.15}$$

Eqn. (2.15) is valid for a long-channel transistor in all modes of operation, from weak to strong inversion and from linear to saturation. It also nicely illustrates the symmetry of the EKV model. Indeed, the expression of g_n remains unchanged when swapping q_s and q_d.

In saturation, without accounting for velocity saturation (VS), g_n is then given by replacing $q_d = 0$

$$g_n \cong \frac{2}{3} \cdot q_s \cdot \frac{q_s + 3/4}{q_s + 1} = \begin{cases} \frac{2}{3}q_s & \text{in strong inversion } (q_s \gg 1) \\ \frac{1}{2}q_s & \text{in weak inversion } (q_s \ll 1). \end{cases} \tag{2.16}$$

In weak inversion, $q_s, q_d \ll 1$ and the normalized thermal noise conductance given by (2.15) simplifies to

$$g_n \cong \frac{q_s + q_d}{2}. \tag{2.17}$$

In strong inversion, $q_s, q_d \gg 1$ and the normalized thermal noise conductance given by (2.15) simplifies to

$$g_n \cong \frac{2}{3} \cdot \frac{q_s^2 + q_sq_d + 4q_d^2}{q_s + q_d}. \tag{2.18}$$

We now will look at the impact of short-channel effects and mainly velocity saturation on the drain current thermal noise.

2.2 Short-channel (with VS)

As the drain voltage of a short-channel transistor biased in stong inversion is increased, at some point the longitudinal electric field E_x becomes equal to a critical field E_c and the drift velocity at the drain end of the channel starts to saturate. Since the drift velocity cannot increase anymore, if the gate voltage is increased a saturation charge builds up close to the drain in order to sustain the drain current despite the saturated velocity. The charge at the drain does not reduce to zero like it would for a long-channel transistor where E_x remains smaller than E_c avoiding any VS. This larger charge at the drain on one hand produces more noise but on the other since the mobility is strongly reduced it impact on the drain current fluctations is mitigated. In reality, there are many short-channel effects that influence the thermal noise as discussed in [4] [7]. In this notebook, we only will consider the effect of VS, ignoring the others. This will allow us to derive a simple empirical model which is very useful for circuit design. A similar approach was already sketched in [8] [7].

In order to obtain an expression valid in all regions of operation, we can proceed in the same way as for deriving the drain current. To obtain an expression of the drain current valid in all regions of operation, we can account for the effect of velocity saturation in strong inversion by replacing q_d by $q_{d_{sat}}$ in the strong inversion part of the current expression and neglecting q_d compared to q_s in the weak inversion part. This allows to have the correct long-channel expression in weak inversion which is not affected by VS. This results in

$$i_{d_{sat}} = q_s^2 - q_{d_{sat}}^2 + q_s, \tag{2.19}$$

where $q_{d_{sat}}$ is the normalized charge that is imposed at the drain because of VS. It depends on q_s and therefore the gate voltage according to

$$q_{d_{sat}} = \frac{1}{\lambda_c} \cdot \left[\sqrt{1 + \lambda_c^2 \left(q_s^2 + q_s\right)} - 1\right] = \frac{\lambda_c \left(q_s^2 + q_s\right)}{1 + \sqrt{1 + \lambda_c^2 \left(q_s^2 + q_s\right)}}. \tag{2.20}$$

Proceeding in the same way for the thermal noise conductance, we replace q_d by $q_{d_{sat}}$ in the part $4(q_s^3 - q_d^3) \cong 4(q_s^3 - q_{d_{sat}}^3)$ corresponding to strong inversion in (2.11) and neglecting q_d in the part $3(q_s^2 - q_d^3) \cong 3q_s^2$ corresponding to weak inversion in (2.11). This leads to

$$g_{n_{sat}} = \frac{1}{i_{d_{sat}}} \cdot \frac{4q_s^3 - 4q_{d_{sat}}^3 + 3q_s^2}{6} \tag{2.21}$$

Replacing $i_{d_{sat}}$ in (2.21) by (2.19) results in

$$g_{n_{sat}} = \frac{1}{6} \cdot \frac{4q_s^3 - 4q_{d_{sat}}^3 + 3q_s^2}{q_s^2 - q_{d_{sat}}^2 + q_s}. \tag{2.22}$$

Eqn. (2.22) gives the correct asymptote $q_s/2$ in weak inversion. However the asymptote in strong inversion is $(1 - \lambda_c/4)\, q_s$ instead of q_s. We can modify (2.22) slightly to get the correct asymptotes in both weak and strong inversion according to

$$g_{n_{sat}} = \frac{1}{6} \cdot \frac{4(q_s^2 + q_s\, q_{d_{sat}} + q_{d_{sat}}^2) + 3q_s}{q_s + q_{d_{sat}} + 1}. \tag{2.23}$$

The normalized thermal noise conductance in strong inversion and saturation including VS simplifies to

$$g_{n_{sat}} \cong \frac{2}{3} \cdot \frac{q_s^2 + q_s q_{d_{sat}} + 4q_d sat^2}{q_s + q_{d_{sat}}}. \tag{2.24}$$

where $q_{d_{sat}}$ is given by (2.20).

In very strong inversion under heavy VS ($\lambda_c\, q_s \gg 1$), $q_{d_{sat}}$ tends to q_s and (2.24) reduces to

$$g_{n_{sat}} \cong q_s \text{ for } q_s \gg 1. \tag{2.25}$$

3 Thermal noise parameter δ_n

3.1 Definition

Several thermal noise factors can be defined according to the definitions introduced initially by van der Ziel [9]. The *thermal noise parameter (TNP)* δ_n is defined as [7] [2] [10]

$$\boxed{\delta_n \triangleq \frac{G_n}{G_{dso}} = \frac{g_n}{g_{dso}}}, \tag{3.1}$$

where G_{dso} is the drain-to-source conductance at $V_{DS} = 0$ and g_{dso} its normalized form

$$g_{dso} \triangleq \frac{G_{dso}}{G_{spec}} = g_{md} = g_{ms} = q_s, \tag{3.2}$$

where g_{ms} and g_{md} are the normalized source and drain transconductances defined by

$$g_{ms} \triangleq \frac{G_{ms}}{G_{spec}} = -\frac{\partial i_d}{\partial v_s} = -\frac{\partial i_d}{\partial q_s} \cdot \frac{\partial q_s}{\partial v_s}, \tag{3.3}$$

$$g_{md} \triangleq \frac{G_{md}}{G_{spec}} = \frac{\partial i_d}{\partial v_d} = -\frac{\partial i_d}{\partial q_d} \cdot \frac{\partial q_d}{\partial v_d}, \tag{3.4}$$

$$g_m \triangleq \frac{G_m}{G_{spec}} = \frac{i_d}{v_g} = \frac{g_{ms} - g_{md}}{n}. \tag{3.5}$$

> **Important**
>
> The δ_n parameter shows how much the thermal noise of the active device deviates from the value it takes when it operates as a passive resistor of conductance G_{dso}.

Since in the linear region (i.e. for $V_{DS} = 0$) the noise conductance G_n is equal to the channel conductance G_{dso}, the noise parameter δ_n is then equal to unity. In saturation, δ_n is equal to

$$\delta_{n_{sat}} \triangleq \frac{g_{n_{sat}}}{G_{dso}} = \frac{g_{n_{sat}}}{g_{dso}} \tag{3.6}$$

where $g_{n_{sat}}$ and $g_{n_{sat}}$ are the values of the thermal conductance in saturation.

> **Note**
>
> Note that Van der Ziel initially used γ for the thermal noise parameter defined by (3.1) and α for the noise excess factor defined by (4.1) [9]. The most important noise excess factor from a circuit design point of view is the one given by (4.1), which has been called γ in many other circuit related paper instead of α as it was defined initially by Van der Ziel in [9]. We will keep the circuit design definition of γ_n and rename the original Van der Ziel's γ as δ_n.

3.2 Long-channel (without VS)

Since $g_{dso} = q_s$, the thermal noise parameter δ_n is given by

$$\delta_n \triangleq \frac{g_n}{g_{dso}} = \frac{1}{6} \cdot \frac{4q_s^2 + 3q_s + 4q_s q_d + 3q_d + 4q_d^2}{q_s(q_s + q_d + 1)}, \tag{3.7}$$

which has the following asymptotes

$$\delta_n \cong \begin{cases} 1 & \text{in the linear region } (q_s = q_d) \\ \delta_{n_{sat}} = \frac{1}{6} \cdot \frac{4q_s+3}{q_s+1} & \text{in saturation } (q_s \gg q_d). \end{cases} . \tag{3.8}$$

In saturation without VS we have

$$\delta_{n_{sat}} \cong \frac{1}{6} \cdot \frac{4q_s + 3}{q_s + 1} = \begin{cases} \frac{2}{3} & \text{in strong inversion } (q_s \gg 1) \\ \frac{1}{2} & \text{in weak inversion } (q_s \ll 1). \end{cases} \tag{3.9}$$

In strong inversion, g_n can be approximated by (2.18) leading to

$$\delta_{n(SI)} \cong \frac{2}{3} \cdot \frac{q_s^2 + q_s q_d + q_d^2}{q_s\,(q_s + q_d)} = \frac{2}{3} \cdot \left[1 + \frac{(q_d/q_s)^2}{1 + q_d/q_s}\right]. \tag{3.10}$$

For a long-channel transistor in saturation, $q_d = 0$ when $v_d = v_p$ and $\delta_{(SI)} \cong \frac{2}{3}$.

3.3 Short-channel (with VS)

The thermal noise parameter is plotted versus v_d in Figure 3.1. For a long channel transistor biased in strong inversion ($v_p = 40$ in Figure 3.1), δ_n ranges from 1 when $v_d = 0$ to 2/3 when $q_d = 0$ as $v_d = v_p$. When VS is included, q_d cannot go to zero and is clamped at $q_{d_{sat}}$ as $v_d = v_{d_{sat}}$. δ_n is then also clamped to the value it takes for $v_d = v_{d_{sat}}$ or $q_d = q_{d_{sat}}$.

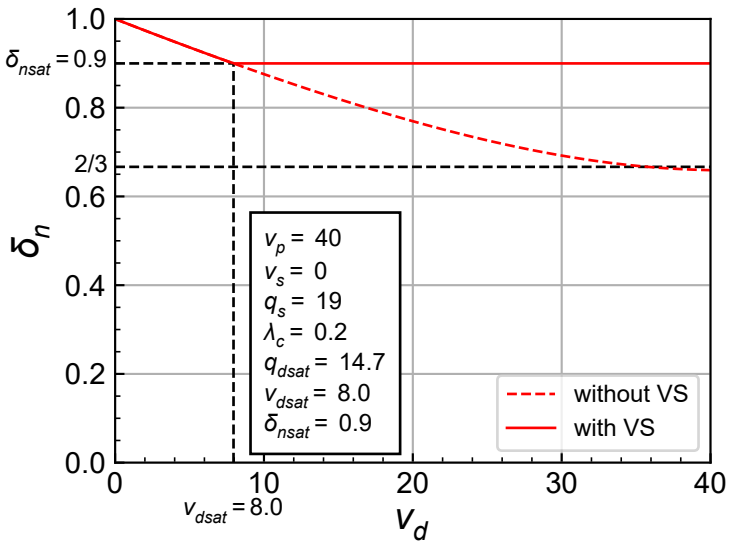

Figure 3.1: Thermal noise parameter δ_n versus drain voltage v_d with and without VS.

We can obtain the value of δ_n in saturation including the effect of VS from (2.23)

$$\delta_{n_{sat}} = \frac{g_{n_{sat}}}{q_s} = \frac{1}{6} \cdot \frac{4(q_s^2 + q_s\, q_{d_{sat}} + q_{d_{sat}}^2) + 3q_s}{q_s(q_s + q_{d_{sat}} + 1)}, \tag{3.11}$$

where $q_{d_{sat}}$ is given by (2.20).

In weak inversion, $q_s \ll 1$ and (3.11) reduces to 1/2 as expected, because VS has no impact in weak inversion.

For a short-channel transistor in strong inversion including VS, (3.11) reduces to

$$\delta_{n_{sat(SI)}} \cong \frac{2}{3} \cdot \frac{q_s^2 + q_s q_{d_{sat}} + q_{d_{sat}}^2}{q_s + q_{d_{sat}}} = \frac{2}{3} \cdot \left[1 + \frac{(q_{d_{sat}}/q_s)^2}{1 + q_{d_{sat}}/q_s}\right]. \tag{3.12}$$

As shown below, in strong inversion ($q_s \gg 1$), $q_{d_{sat}}$ tends to q_s

$$q_{d_{sat}} \cong q_s \text{ for } q_s \gg 1, \tag{3.13}$$

and hence $g_{n_{sat(SI)}}$ in strong inversion with VS also tends to q_s and therefore $\delta_{n_{sat}}$ tends to unity.

The thermal noise parameters in saturation is plotted versus the inversion coefficient IC in Figure 3.2 for different values of λ_c. We see that for $\lambda_c = 0.5$, $\delta_{n_{sat}}$ tends to unity for $IC \gg 1$.

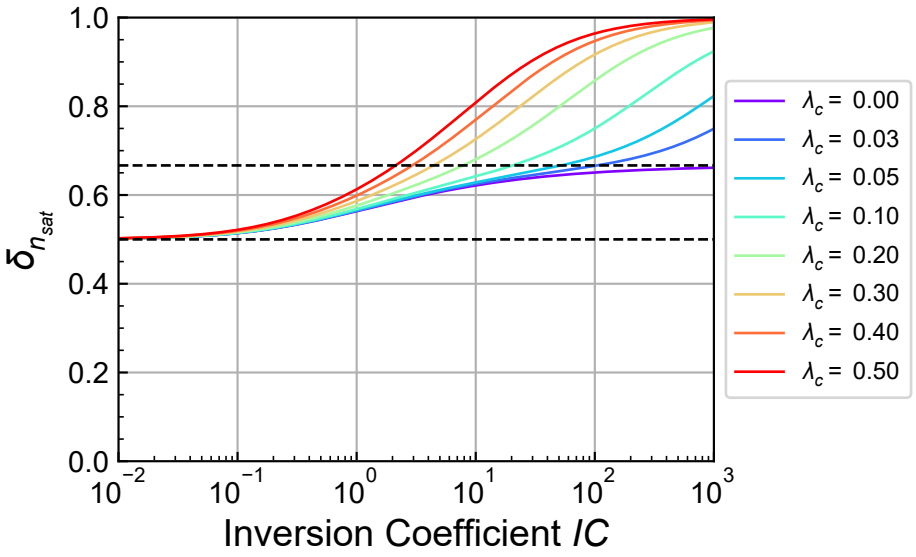

Figure 3.2: Thermal noise parameter $\delta_{n_{sat}}$ versus inversion coefficient IC including short-channel effects.

4 Thermal noise excess factor γ_n

4.1 Definition

Note that the δ_n thermal noise parameter compares the thermal noise conductance evaluated at a given operating point to that of the MOSFET when it is biased as resistor with $V_{DS} = 0$ having a condcutance G_{dso}. This is not very usefull for circuit design and is mostly used for modeling comparing the actual noise to the noise produced by a resistor having a conductance G_{dso}. For circuit design, it is more useful to define another figure-of-merit γ_n, named the *thermal noise excess factor (TNEF)* and defined as [7] [2] [10]

$$\boxed{\gamma_n \triangleq \frac{G_n}{G_m} = \frac{g_n}{g_m}}. \tag{4.1}$$

where g_m is the normalized gate transconductance defined by (3.5).

> **!** The TNEF γ_n as a figure-of-merit (FoM)
>
> The TNEF γ_n represents how much noise is generated in the drain current for a given transconductance.

Contrary to the TNP δ_n, the noise conductance and the gate transconductance used in the definition (4.1) are evaluated *at the same operating point*. γ_n has a direct impact on the noise performance of circuits. The smaller γ_n, the better the noise performance of the circuit.

> **i** TNEF γ_n in the linear region
>
> Note that γ_n can become quite large when the device operates in the linear region, i.e. for $V_{DS} < V_P - V_S \cong (V_G - V_{T0})/n - V_S$. Indeed, in this region, the gate transconductance gets smaller as the drain voltage decreases, but the thermal noise conductance does not decrease, resulting in a degradation of the TNEF γ_n. At the limit when V_{DS} becomes zero, the transconductance becomes zero and γ_n tends to infinity. In practice, the TNEF γ_n is mostly used for transistors biased in saturation.

The TNP δ_n and the TNEF γ_n are related by

$$\gamma_n = \frac{G_n}{G_{dso}} \cdot \frac{G_{dso}}{G_m} = \delta_n \cdot \frac{G_{dso}}{G_m} = \delta_n \cdot n \cdot \frac{G_{dso}}{G_{ms} - G_{md}} = \delta_n \cdot n \cdot \frac{g_{dso}}{g_{ms} - g_{md}}, \tag{4.2}$$

which in saturation reduces to

$$\gamma_{n_{sat}} = \frac{g_{n_{sat}}}{g_{m_{sat}}} = n \cdot \frac{g_{n_{sat}}}{g_{ms}}, \tag{4.3}$$

4.2 Long-channel (without VS)

In saturation without VS, $q_d = 0$ and $g_{n_{sat}}$ and $g_{m_{sat}}$ reduce to

$$g_{n_{sat}} \cong q_s \cdot \frac{2}{3} \cdot \frac{q_s + 3/4}{q_s + 1}, \tag{4.4}$$

$$g_{m_{sat}} = \frac{g_{ms}}{n} \cong \frac{q_s}{n}. \tag{4.5}$$

The TNEF in saturation $\gamma_{n_{sat}}$ in then given by

$$\gamma_{n_{sat}} \cong \frac{2n}{3} \cdot \frac{q_s + 3/4}{q_s + 1} = \begin{cases} \frac{2n}{3} & \text{in strong inversion } (q_s \gg 1) \\ \frac{n}{2} & \text{in weak inversion } (q_s \ll 1). \end{cases} \tag{4.6}$$

The thermal noise excess factor for a long-channel transistor is plotted versus the inversion coefficient in Figure 4.1. The red curve assumes that the slope factor is constant, which is not exactly the case as shown by the blue dashed line. However, we will consider that n remains constant and independent of the inversion coefficient.

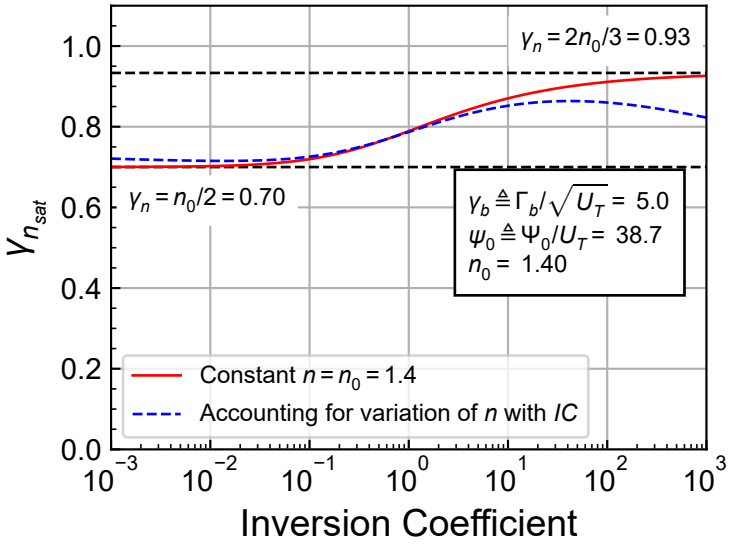

Figure 4.1: Thermal noise excess parameter γ_n versus inversion coefficient IC.

4.3 Short-channel (with VS)

For short-channel devices in saturation, we need to account for VS

$$\gamma_{n_{sat}} = \frac{g_{n_{sat}}}{g_{m_{sat}}} = n \cdot \frac{g_{n_{sat}}}{g_{ms_{sat}}}, \tag{4.7}$$

where the thermal noise conductance $g_{n_{sat}}$ is given by (2.23) and the normalized source transconductance in saturation $g_{ms_{sat}}$ and accounting for VS is given by

$$g_{ms_{sat}} = \frac{q_s}{\sqrt{1 + \lambda_c^2 \left(q_s^2 + q_s\right)}}. \tag{4.8}$$

The thermal noise excess factor in saturation is plotted version the inversion coefficient and represented by circles in Figure 4.2 for different values of λ_c. We see that $\gamma_{n_{sat}}$ increases dramatically with IC for $\lambda_c = 0.3$. Note that this happens for advanced technologies for which it becomes more an more difficult to reach inversion coefficient as high as 100 because of voltage scaling. So the TNEF increases to about 3.5 for $IC = 40$ which is consistent with measurements shown below.

The TNEF is plotted with a linear x-axis for the same values of λ_c in Figure 4.3 which highlights that $\gamma_{n_{sat}}$ actually increases linearly with IC in strong inversion. This is discussed in more details below.

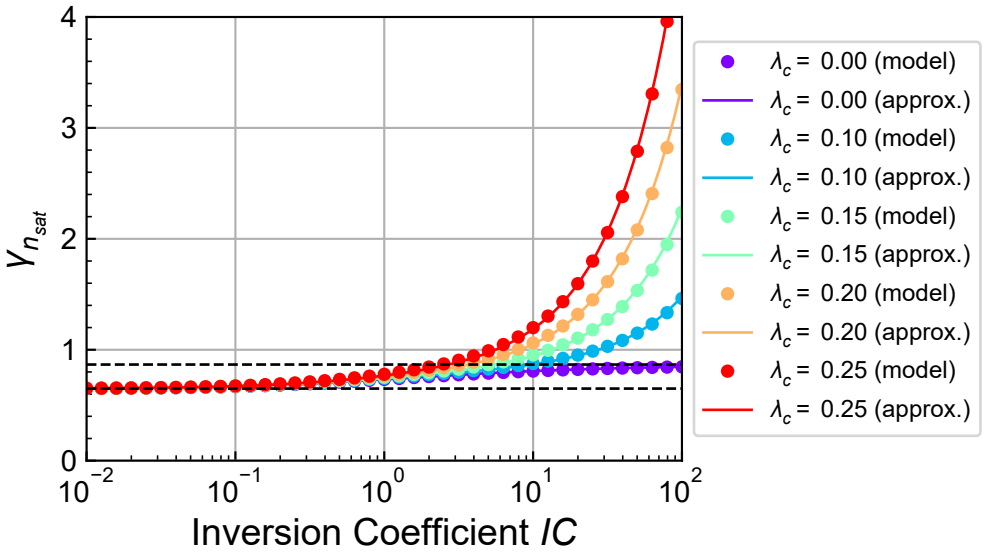

Figure 4.2: Thermal noise excess factor $\gamma_{n_{sat}}$ versus inversion coefficient IC including short-channel effects.

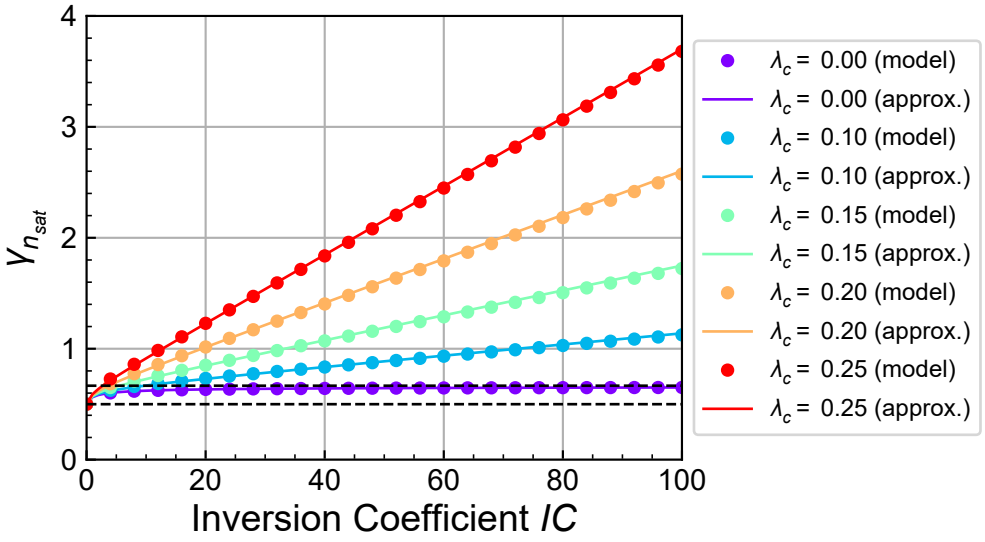

Figure 4.3: Thermal noise excess factor $\gamma_{n_{sat}}$ versus inversion coefficient IC including short-channel effects.

4.4 Strong inversion approximation

In strong inversion and saturation $g_{n_{sat}}$ and $g_{m_{sat}}$ can be approximated by

$$g_{n_{sat}} \cong \frac{2}{3} \cdot \frac{q_s^2 + q_s\, q_{d_{sat}} + 4 q_d sat^2}{q_s + q_{d_{sat}}}, \tag{4.9}$$

$$g_{m_{sat}} = \frac{g_{ms}}{n} \cong \frac{q_s}{n\sqrt{1 + (\lambda_c\, q_s)^2}} \tag{4.10}$$

In very strong inversion under heavy VS, i.e. for $\lambda_c\, q_s \gg 1$, (4.9) tend to

$$g_{n_{sat}} \cong q_s, \tag{4.11}$$

$$g_{m_{sat}} = \frac{1}{n\,\lambda_c}. \tag{4.12}$$

The thermal noise excess factor in very strong inversion and under heavy VS has the following asymptote for $\lambda_c\, q_s \gg 1$

$$\gamma_{n_{sat}} \cong n \cdot \lambda_c \cdot q_s. \tag{4.13}$$

We can also express this asymptote in terms of the inversion coefficient IC. Indeed, for $1 \ll \lambda_c\, q_s$, $i_{d_{sat}}$ simplifies to $i_{d_{sat}} = IC \cong 2q_s/\lambda_c$. Hence $q_s \cong \lambda_c/2 \cdot i_{d_{sat}} = \lambda_c/2 \cdot IC$. Therefore in very strong inversion under heavy VS, as illustrated in Figure 4.3, the TNEF becomes proportional to IC according to

$$\gamma_{n_{sat}} \cong \frac{n}{2} \cdot \lambda_c^2 \cdot IC. \tag{4.14}$$

4.5 Weak inversion approximation

In weak inversion $q_d \ll 1$ and $q_s \ll 1$ and g_n simplifies to

$$g_n \cong \frac{q_s + q_d}{2} \quad \text{(weak inversion)} \tag{4.15}$$

which in saturation $q_d \ll q_s \ll 1$ simplifies to

$$g_{n_{sat}} \cong \frac{q_s}{2} \quad \text{(weak inversion and saturation)}. \tag{4.16}$$

On the other hand $g_{m_{sat}}$ is given by

$$g_{m_{sat}} \cong \frac{g_{ms_{sat}}}{n} = \frac{q_s}{n}. \tag{4.17}$$

The thermal noise excess factor is therefore constant and equal to

$$\gamma_{n_{sat}} \cong \frac{n}{2} \quad \text{(weak inversion and saturation)}. \tag{4.18}$$

4.6 Approximation valid from weak to strong inversion

The TNEF can be approximated by

$$\gamma_{n_{sat}} \cong \gamma_{n_{sat}}|_{\text{no VS}} \cdot \left(1 + \frac{3}{4} \cdot \lambda_c^2 \cdot IC\right), \tag{4.19}$$

where

$$\gamma_{n_{sat}}|_{\text{no VS}} = n \cdot \delta_{n_{sat}}, \tag{4.20}$$

with $\delta_{n_{sat}}$ given by (3.11). Eqn. (4.19) has the correct asymptotes, because in weak inversion $\frac{3}{4} \cdot \lambda_c^2 \cdot IC \ll 1$ and hence

$$\gamma_{n_{sat}} \cong \gamma_{n_{sat}}|_{\mathsf{no\ VS}} = \frac{n}{2}. \tag{4.21}$$

On the other hand, in strong inversion $1 \ll \frac{3}{4} \cdot \lambda_c^2 \cdot IC$, resulting in

$$\gamma_{n_{sat}} \cong \gamma_{n_{sat}}|_{\mathsf{no\ VS}} \cdot \frac{3}{4} \cdot \lambda_c^2 \cdot IC = \frac{2\,n}{3} \cdot \frac{3}{4} \cdot \lambda_c^2 \cdot IC = \frac{n}{2} \cdot \lambda_c^2 \cdot IC. \tag{4.22}$$

Eqn. (4.19) is plotted in Figure 4.2 and Figure 4.3 (represented by lines) and compared to the results from the full expression (represented by circles). We see a very good fit between the approximation (4.19) (lines) and the full expression (4.7) (symbols).

5 Comparison with measurements

In this section, we will compare the simple model of the thermal noise excess factor in saturation $\gamma_{n_{sat}}$ given by (4.19) with measurements made on different devices from various technologies [11], [12]. The slope factor is imposed and the VS parameter λ_c is extracted using simple curve fitting. The results are presented in Figure 5.1. The fit is OK for the 240nm, 180nm and 40nm technologies but there are some discrepancies at low IC for the 120nm and 100nm technologies. However, we have to remember that the model only uses a single parameter namely the VS parameter λ_c.

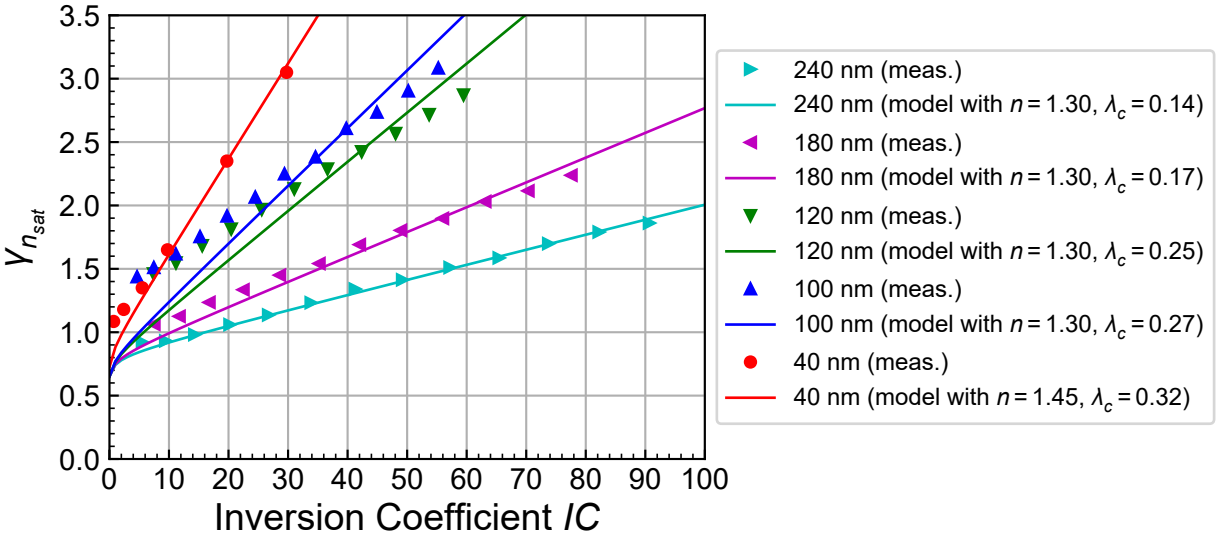

Figure 5.1: Experimental validation of simple TNEF model.

Since the discrepancy appears at low IC, we can modify the model making the value of γ_n in weak inversion, which is normally equal to $n/2$, a fitting parameter. The proposed empirical model is then given by [13]

$$\gamma_{n_{sat}} \cong \gamma_{nwi} \cdot (1 + \alpha_n \cdot IC). \tag{5.1}$$

From the asymptotic behavior in strong inversion given by (4.14), α_n should be equal to

$$\alpha_n = \frac{n}{2\,\gamma_{nwi}} \cdot \lambda_c^2 \cong \frac{n}{2} \cdot \lambda_c^2. \tag{5.2}$$

However, we now will use it as an independent fitting parameter.

The empirical model (5.1) is compared to the same measured data in Figure 5.2 after extraction of parameters γ_{nwi} and α_n by curve fitting. We now see a very good agreement between the simple empirical model (5.1) and the measured data. We can observe that the fitting parameter γ_{nwi} is getting larger than the theoretical value $n/2$. However it remains close to one.

We can extract the corresponding VS parameter from (5.2) resulting in

$$\lambda_c = \sqrt{\frac{2\,\gamma_{nwi}\,\alpha_n}{n}} \cong \sqrt{\frac{2\,\alpha_n}{n}}. \tag{5.3}$$

The fitting parameters γ_{nwi} and α_n, the imposed slope factor n and the corresponding extracted value of λ_c are presented in Table 5.1. Figure 5.3 shows that α_n is scaling as $/1/L$.

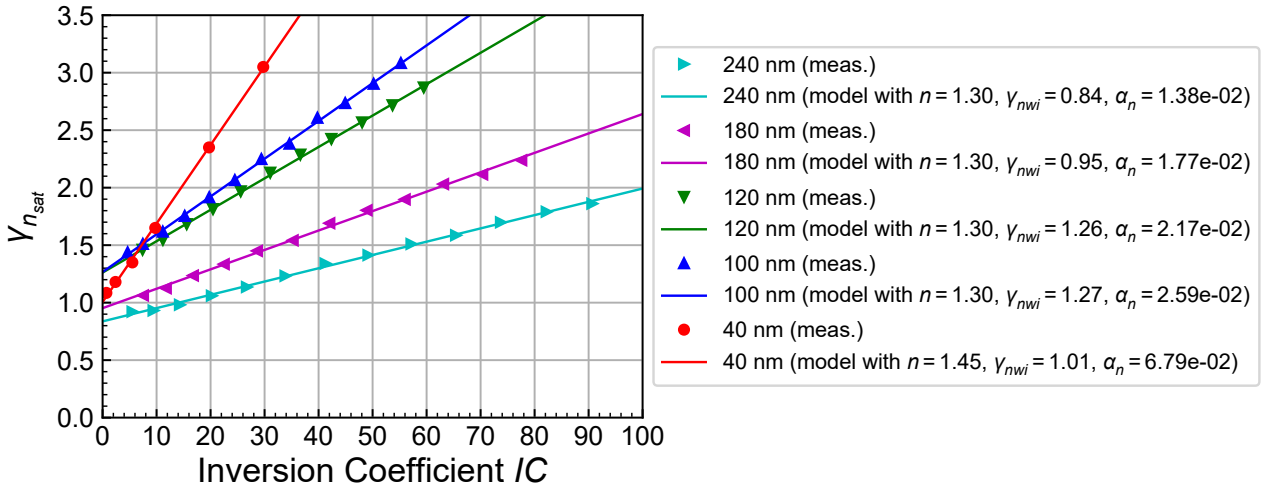

Figure 5.2: Experimental validation of the TNEF empirical model.

Table 5.1: Fitting parameters.

Techno	γ_{nwi}	α_n	n	λ_c
240nm	0.837	0.0138	1.3	0.133
180nm	0.952	0.0177	1.3	0.161
120nm	1.261	0.0217	1.3	0.205
100nm	1.266	0.0259	1.3	0.225
40nm	1.005	0.0679	1.45	0.307

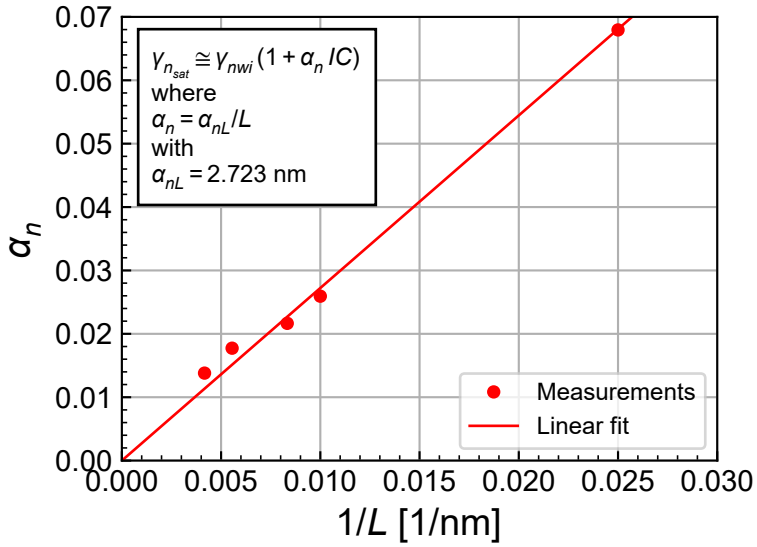

Figure 5.3: Scaling of the α_n parameter with $1/L$.

6 Application to LNA design

6.1 Input-referred thermal noise resistance

The input-referred thermal noise resistance is defined as

$$R_n \triangleq \frac{\gamma_{n_{sat}}}{g_{m_{sat}}} \tag{6.1}$$

and its normalized form is given by

$$r_n \triangleq G_{spec} \cdot R_n = \frac{\gamma_{n_{sat}}}{g_{m_{sat}}}. \tag{6.2}$$

Without VS, $\gamma_{n_{sat}}$ remains constant and $g_{m_{sat}}$ increases proportionally to the inversion coefficient IC in weak inversion and then as $\sqrt{IC}$ in strong inversion. Therefore, the term $\gamma_{n_{sat}}/g_{m_{sat}}$ decreases with respect to IC improving the noise performance. When VS is present, $\gamma_{n_{sat}}$ depends on IC and increases as $\alpha_n \cdot IC$ in strong inversion and saturation whereas $g_{m_{sat}}$ saturates to its maximum value $G_{spec}/(n\lambda_c)$. The $\gamma_{n_{sat}}/g_{m_{sat}}$ ratio therefore increases now in strong inversion and saturation. The normalized $\gamma_{n_{sat}}/g_{m_{sat}}$ ratio is then given by

$$r_n = \frac{\gamma_{n_{sat}}}{g_{m_{sat}}} \cong \frac{n}{2} \cdot \lambda_c^2 \cdot IC \cdot n\,\lambda_c = \frac{n^2}{2} \cdot \lambda_c^3 \cdot IC \quad \text{in SI and sat. with VS.} \tag{6.3}$$

In weak inversion the situation is different since $\gamma_{n_{sat}} \cong \gamma_{nwi} \cong 1$ and $g_{m_{sat}} \propto IC$. The term $\gamma_{n_{sat}}/g_{m_{sat}}$ is now decreasing as $1/IC$ in weak inversion and saturation. In normalized form this gives

$$r_n = \frac{\gamma_{n_{sat}}}{g_{m_{sat}}} \cong \gamma_{nwi} \cdot \frac{n}{IC} = \frac{n}{IC} \quad \text{in WI and sat.} \tag{6.4}$$

This means that there is an optimum value of IC for which the term $\gamma_{n_{sat}}/g_{m_{sat}}$ reaches a minimum. An approximation of this optimum inversion coefficient is found by equating the two asymptotes and solving for IC. This results in

$$IC_{opt} \cong \sqrt{\frac{2}{n\,\lambda_c^3}}. \tag{6.5}$$

Note that this optimum IC only depends on λ_c according to (6.5) and is often in the upper side of moderate inversion.

The normalized input-referred thermal noise resistance r_n in saturation is plotted versus the inversion coefficient IC for a 40nm transistor in Figure 6.1.

For a common-source low-noise amplifier (LNA) at RF we need to add the transistor gate resistance R_G to the input-referred thermal noise resistance according to

$$R_n \cong \frac{\gamma_n}{G_m} + R_G. \tag{6.6}$$

Although this gate resistance is usually small, it plays a fundamental role for noise at RF particularly in advanced CMOS technologies for which it has significantly increased after the the introduction of high-K dieletric and metal gates.

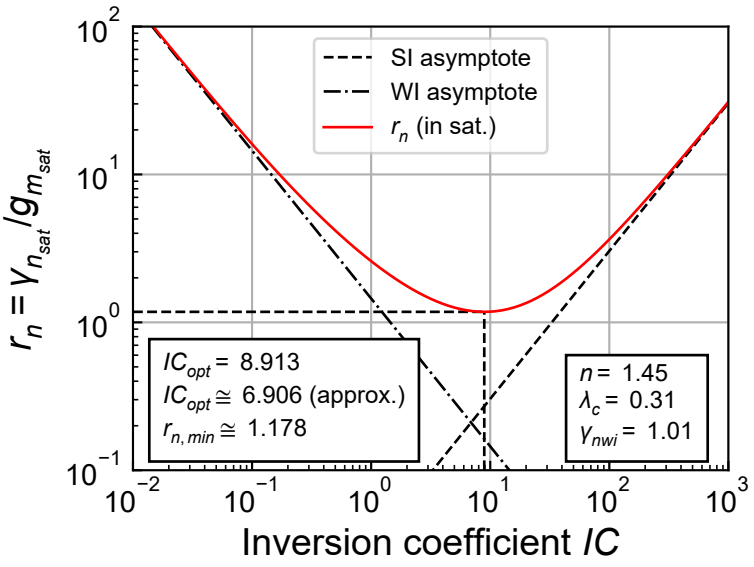

Figure 6.1: Normalized input-referred thermal noise resistance versus IC including VS.

The input-referred noise resistance R_n has been measured on an RF transistor from a 40nm bulk CMOS technology at 10 and 14 GHz [12]. The measured R_n normalized to $Z_0 = 50\,\Omega$ are plotted in Figure 6.2 versus the inversion coefficient IC and compared to the analytical model taking the values of γ_{nwi} and α_n extracted above for the same 40nm device. The good match between the model and the experimental data validates this simple model. The optimum inversion coefficient for which R_n is minimum is about equal to 10.

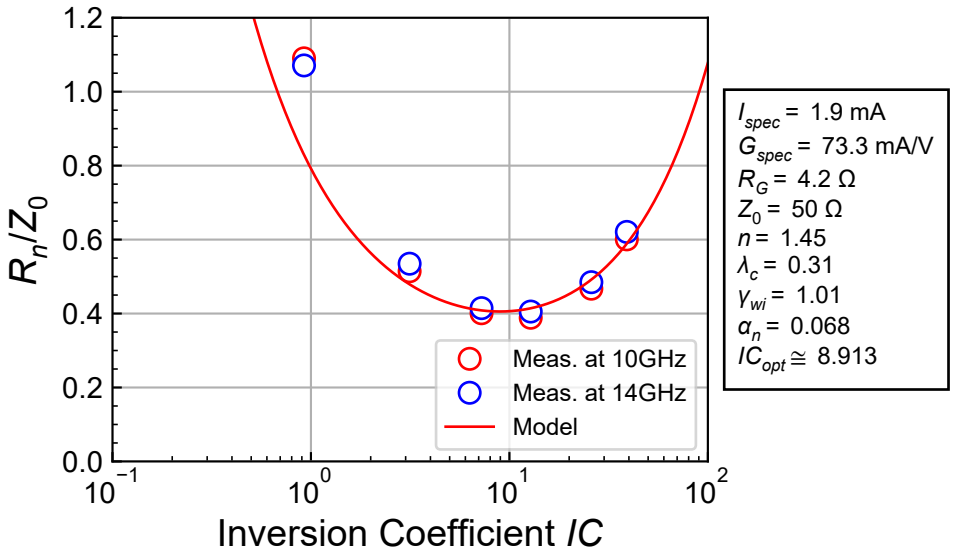

Figure 6.2: Measured input-referred noise resistance versus IC.

6.2 Minimum noise figure

It can be shown that the minimum noise factor accounting for the effects of the gate resistance and the induced-gate noise (but without the correlation) is given by [2]

$$F_{min} \cong 1 + 2\frac{\gamma_{n_{sat}}}{g_{m_{sat}}}\,\omega\,C_{GS}\,\sqrt{\alpha_G + b_n}, \tag{6.7}$$

where C_{GS} is the gate-to-source capacitance, $b_n = 2/(5n^2)$ and α_G is the thermal noise contribution of the gate resistance normalized to that of the channel

$$\alpha_G \triangleq \frac{R_G}{\gamma_{n_{sat}}/g_{m_{sat}}}. \tag{6.8}$$

The minimum noise figure NF_{min} has been measured on the same device at 10 GHz and 14 GHz and is plotted versus the inversion coefficient in Figure 6.3. The minimum noise figure NF_{min} is sensitive to many parameters and it is therefore not that easy to get a simple but accurate model. We can consider therefore that the match between the experimental data and the simple model is acceptable accounting for the simplicity of the proposed model. The optimum inversion coefficient providing the minimum NF_{min} is again close 10.

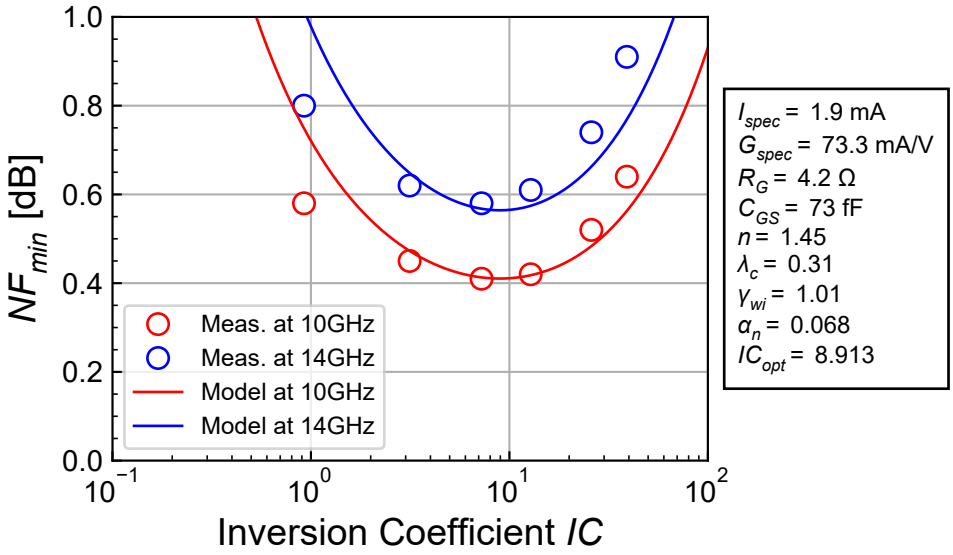

Figure 6.3: Minimum noise figure measured at 10 and 14 GHz versus IC.

7 Conclusion

This notebook has presented a simple model of the thermal noise of short-channel transistors. It has been shown that the thermal noise excess factor in saturation accounting for short-channel effects (actually velocity saturation) actually increases proportionnally to the inversion coefficient IC in strong inversion while the impact of velocity saturation in weak inversion remains negligible. The proposed model has been validated with experimental data from various CMOS bulk technologies down to 40nm. The model shows that the input-referred thermal noise resistance of a common-source transistor shows a minimum in the upper side of moderate inversion. The input-referred noise resistance of a common-source transistor has been measured at 10 and 14 GHz and confirms the existence of a minimum. The model including an additional gate resistance matches the measured input-referred noise resistance very well. A model of the minimum noise figure has been proposed and has been successfully compared to measurements made at 10 and 14 GHz. The proposed model is simple enough for correctly choosing the best operating point choosing the optimum inversion coefficient providing a minimum input-referred noise resistance and minimum noise figure.

References

[1] C. C. Enz and G. C. Temes, "Circuit techniques for reducing the effects of op-amp imperfections: autozeroing, correlated double sampling, and chopper stabilization," *Proceedings of the IEEE*, vol. 84, no. 11, pp. 1584–1614, 1996.

[2] C. C. Enz and E. A. Vittoz, *Charge-Based MOS Transistor Modeling - The EKV Model for Low-Power and RF IC Design*, 1st ed. John Wiley, 2006.

[3] F. M. Klaassen and J. Prins, "Thermal Noise of MOS Transistors," *Philips Res. Repts*, vol. 22, pp. 505–514, 1967.

[4] A. S. Roy and C. C. Enz, "Compact Modeling of Thermal Noise in the MOS Transistor," *IEEE Trans. Electron Devices*, vol. 52, no. 4, pp. 611–614, 2005.

[5] C. Enz, F. Chicco, and A. Pezzotta, "Nanoscale MOSFET Modeling: Part 1: The Simplified EKV Model for the Design of Low-Power Analog Circuits," *IEEE Solid-State Circuits Magazine*, vol. 9, no. 3, pp. 26–35, 2017.

[6] C. Enz, F. Chicco, and A. Pezzotta, "Nanoscale MOSFET Modeling: Part 2: Using the Inversion Coefficient as the Primary Design Parameter," *IEEE Solid-State Circuits Magazine*, vol. 9, no. 4, pp. 73–81, 2017.

[7] A. S. Roy and C. C. Enz, "Compact Modeling of Thermal Noise in the MOS Transistor," in *Proceeding of the international conference on mixed design of integrated circuits and systems (MIXDES)*, Szczecin, Poland, 2004, pp. 71–78.

[8] C. C. Enz, "A comprehensive study of thermal noise in the MOS transistor," in *Second international symposium on fluctuations and noise, proc. SPIE 5470, noise in devices and circuits II*, May 2004, pp. 84–95.

[9] A. v. d. Ziel, *Noise in Solid State Devices and Circuits*. John Wiley, 1986.

[10] Y. Cui, G. Niu, Y. Li, S. S. Taylor, Q. Liang, and J. D. Cressler, "On the Excess Noise Factors and Noise Parameter Equations for RF CMOS," in *2007 topical meeting on silicon monolithic integrated circuits in RF systems*, 2007, pp. 40–43.

[11] A. Antonopoulos *et al.*, "CMOS Small-Signal and Thermal Noise Modeling at High Frequencies," *IEEE Transactions on Electron Devices*, vol. 60, no. 11, pp. 3726–3733, 2013.

[12] M. A. Chalkiadaki and C. C. Enz, "RF Small-Signal and Noise Modeling Including Parameter Extraction of Nanoscale MOSFET From Weak to Strong Inversion," *IEEE Trans. on Microwave Theory and Techniques*, vol. 63, no. 7, pp. 2173–2184, 2015.

[13] C. Enz, "Simple Expression of the Thermal Noise Excess Factor for LNA Design," in *2022 29th IEEE international conference on electronics, circuits and systems (ICECS)*, 2022, pp. 1–4.

